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Digital Up-Down Converter Using Optimized CIC Filter for Mobile Satellite Services

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Abstract
The digital industry is vivaciously escalating with rising demand for digital based products. A great part of this deals with Digital Signal Processing. Programmable DSPs based on software dependent computation are widely used for baseband processing function such as filtering, frequency shifting, modulation-demodulation, etc. Paper deals with implementation of high performance and real time Digital Up-Down converter with minimum utilization of resources. Digital up converter are used at the transmitter side to shift the frequency from baseband to IF. Digital down converter are used at the receiver side to carry the signal back to the baseband. The whole system is programmed using (Very High Speed Integrated Circuit) hardware description language and synthesize on Stratix-III development board.

Keywords
CIC Filter, NCO, DUC, DDC

I. Introduction

Communication plays a vital role in day to day life to transfer the information. Though there are diverse mode of communication at present, Digital communication is more admired. It is a process of transferring signal in digital format i.e. Bits. a transmitter, channel and receiver are the main block of communication system. DUC and DDC presented in this paper are the part of transmitter and receiver respectively.

A variety of communication systems, which carry immense amounts of data between terminals and end users of many kinds, exist today. Necessitated by the global compliant requisition original equipment manufacturer are expected to provide convergent solutions that accommodate various standards within a single embodiment. Such systems, however achieve the desired convergence with the least expendable resources: hardware silicon real estate and product turn over time [1].

Main motive is to optimize the design to minimize the usage of resources by using fewer components. DUC-DDC have been implemented in the single platform to make the system complete. Using this topology, the network providers have the ability to configure the digital front-end based on demand and integrate all the transmit/receive functionalities into a unified and custom-built hardware platform.

System architecture for the entire design is shown in fig.1. Baseband signal are processed on FPGA platform containing DUC-DDC, where all computation of the digital signal takes place. DUC are used to bring the signal up from base band to IF and DDC is vice-versa.

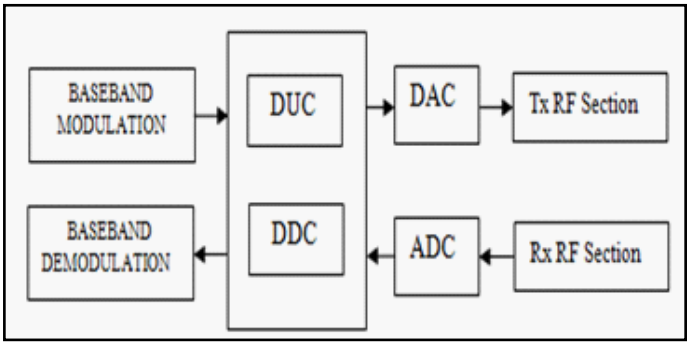

Fig.1 : System Design

II. Proposed Model

A. Transmitter Side

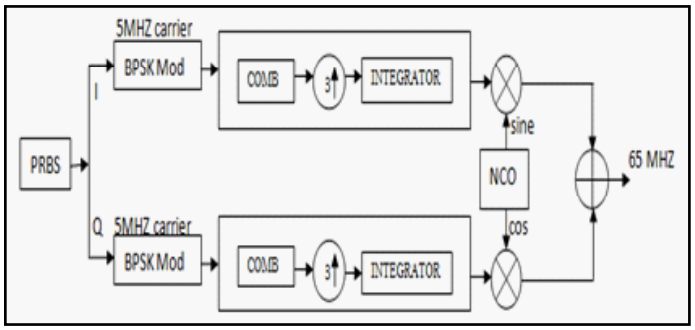

Fig. 2 : Transmitter block

Transmitter side architecture of DUC design is as shown in fig.2. BPSK modulation is carried out using ROM table method. BPSK modulated I and Q having carrier frequency f_c=5MHZ and data rate f_b=250kbps are applied to the CIC filter. The baseband BPSK I and Q having sampling frequency equal to 80Msps is up sampled by 3. Hence, the new sampling frequency becomes 240Msps. DUC having two identical paths one for in phase and another quadrature phase, for that it is also termed as complex DUC.

Up sampled baseband BPSK modulated signal, having sampling frequency equal to 240Msps is multiplied with the Direct Digital Synthesizer's (DDS) output, to turn out the spectrum centre on the desired IF of 65MHZ. Generated output signal have three frequency component with frequencies: 55 , 60 and 65MHZ. According to trigonometry rule shown in equation (1) and (2), linear addition of I and Q signal results into a single sideband signal with suppressed carrier as shown in equation (3).

$$\cos\alpha\cos\beta = \frac{1}{2}(\cos(\alpha-\beta)+\cos(\alpha+\beta)) \quad (1)$$

$$\sin\alpha\sin\beta = \frac{1}{2}(\cos(\alpha-\beta)-\cos(\alpha+\beta)) \quad (2)$$

$$\cos\alpha\cos\beta+\sin\alpha\sin\beta = \frac{1}{2}(2\cos(\alpha+\beta)) \quad (3)$$

B. Receiver side

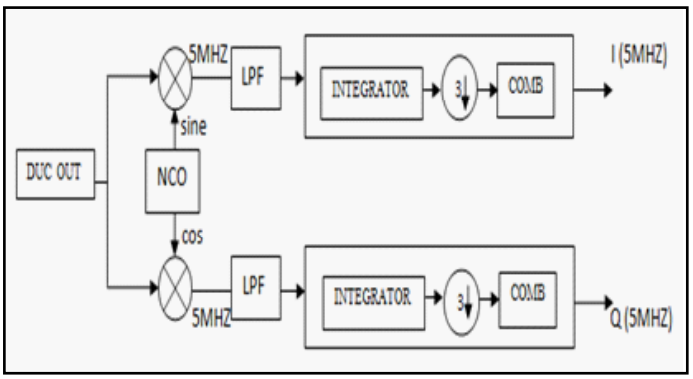

Fig. 3 : Receiver block

DDC chain works exactly opposite to the DUC chain. DDC is required to recover baseband signal from IF signal. DDC converts the signal at the output of ADC, centred at the IF to complex baseband signal without affecting it spectral characteristic. Frequency down shifting of IF signal, having 65MHz is carried out by multiplying it with DDS output to get the baseband signal of 5MHZ. The baseband signal is down sampled by factor 3 to bring it back to the lower sampling frequency at receiver side.

C. NCO

NCO used in the system has Multiplier based architecture. Multiplier based architecture can be implemented with either:

- Logic elements or combinational ALUTs.
- Dedicated multiplier circuitry

Advantage of using Multiplier based NCO architecture is that it uses less memory, which make us eases to implement
Following are the parameters and resource estimation of the NCO used:

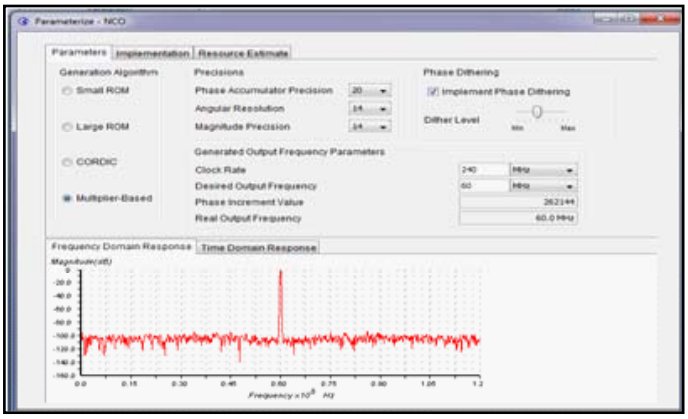

Fig. 4 : Parameter of NCO Mega Core

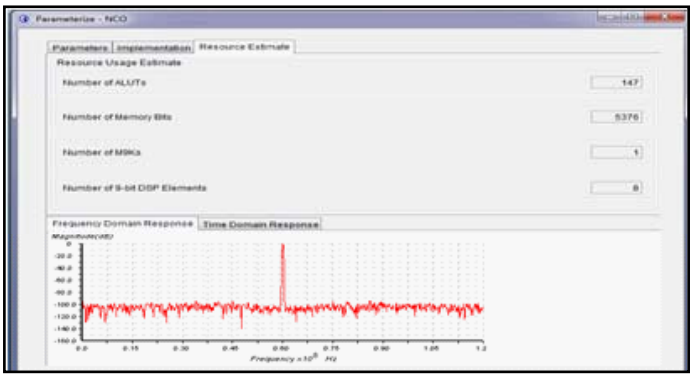

Fig. 5 : Resource utilization of NCO

D. CIC FILTER

CIC filter consists of two elementary units, integrator and combfilter. An integrator is a typical single –pole IIR filter of unity feedback coefficient.

$y(n) = y(n-1) + x(n)$

In Z plane it's given as

$HI(z) = y(z)/x(z) = 1 / (1-z^{-1})$

A comb filter operating at high sampling rate, 'f_s', with a rate change 'R' acts as an odd-symmetric FIR
Filter is described by following equation

$y(n) = x(n) + x (n- RM)$

Here M is deferential delay. It can be any positive integer, usually considers either 1 or 2.The Z plane transfer function is given by

$HC(z) = x(z)/y(z) = [1- z^{-RM}]$

For constructing a CIC filter, one needs to cascade or bind output to input, N integrator slices along with N comb slices. The formed filter could be more simplified with a rate changer. If we drive the comb slice via the rate changer, then we have the following,

$y(n) = x(n) + x (n- M)$

at slower sampling rate f_s/R. By doing this three things are achieved. First constraining or holding back half of the filter thereby increasing its efficiency. Second, reducing the delay units required in comb portion. Third, the crucial arrival, the integrator and comb frame become liberated of the rate change.

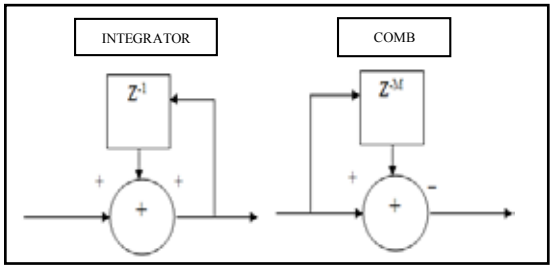

Fig. 5 : Comb and Integrator

In short, CIC decimator frame comprises cascaded *N* integrator slices clocked at f_s, followed by rate change R, and cascaded N comb slices running at . A CIC interpolator would comprise of cascaded *N* comb slices running at, followed by a zero-stuffer, and cascaded *N* integrator slices at f_s.

III. Optimized CIC Filter

A. Optimized CIC Interplation filter

An efficient implementation technique for CIC interpolation is the use of HOLD interpolator. The core structure of CIC filter consists of single stage CIC. Single stage CIC filter is shown in fig.6.

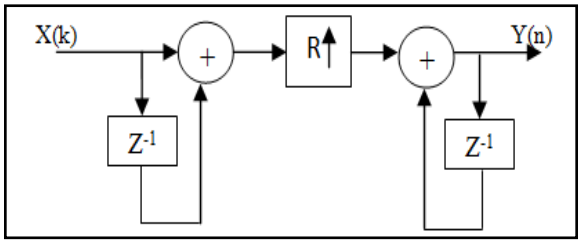

Fig. 6 : Hold Interpolator

Function of innermost single stage interpolator is to hold the input sample for R-1 times the input samples. Thus the core part can be replaced by the hold interpolator. This implementation technique is hardware efficient as usage of adder and delay are reduced.

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Three stage CIC filter with Hold Interpolator is as shown in Fig7.

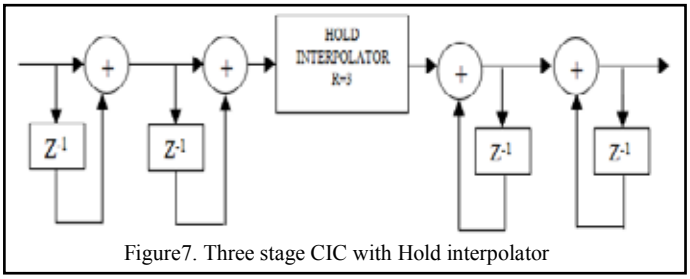

Figure7. Three stage CIC with Hold interpolator

Fig. 7 : Three stage CIC with Hold interpolator

IV. FPGA Implementaiotn

Design has been synthesized on Stratix-III development board. Input is given to the data conversion card of the Stratix-III board. Outputs of the digital oscilloscope are shown in Fig 8 and 9.

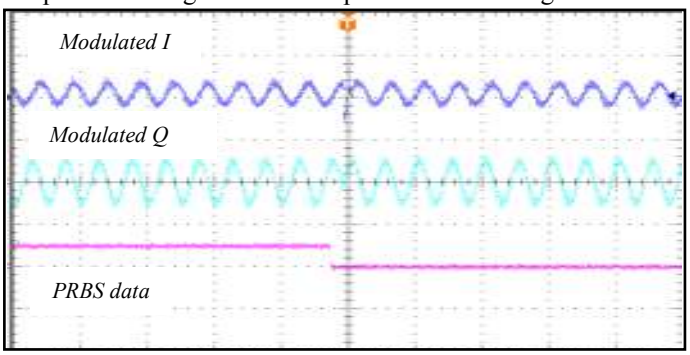

Fig.8 :Modulated sine and cos with sampling 80MHZ.

Input modulated signal is up sampled by 3 using multirate CIC filter. Thus input frequency remains same 5MHZ with sampling increase to 240MHZ.

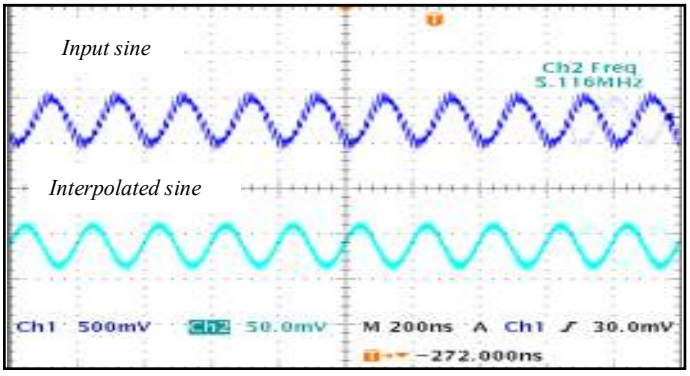

Fig. 9 : Upsampled by 3

Spectrum result of all corresponding stage is shown in fig 10, 11 and 12. Fig 10 shows the spectrum result of modulated I with centre 5MHZ.

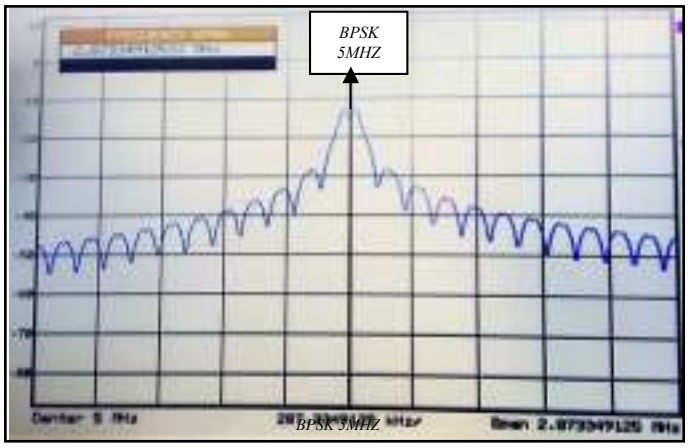

Fig.10 : Spectrum result of BPSK sine with centre 5MHZ

After multiplying with NCO signal, three frequency component of ±5 are obtained. Fig 11 shows the spectrum result of mixer.

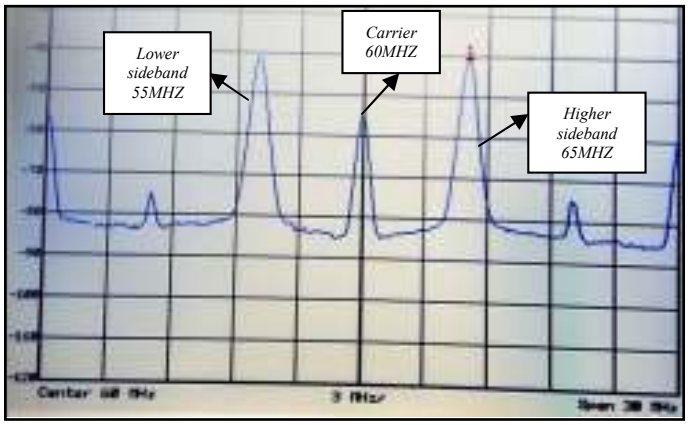

Fig. 11 : Mixer output

By linearly adding the sine and cosine term, only higher sideband is obtained. Fig 12 shows the spectrum result of adder with centre suppressed and having higher band only.

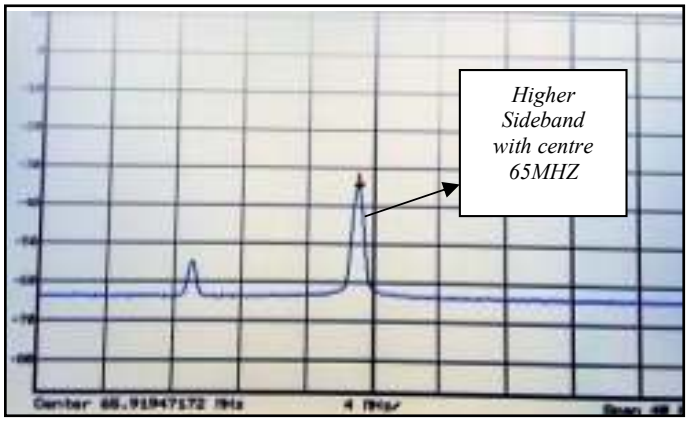

Fig. 12 : Adder output

DDC chain, which includes multiplying with NCO to get the baseband signal back and down sampling by 3, so that further sampling can be done with lower sampling frequency. DDC output of I and Q signal are shown in Fig 13 and 14 resp.

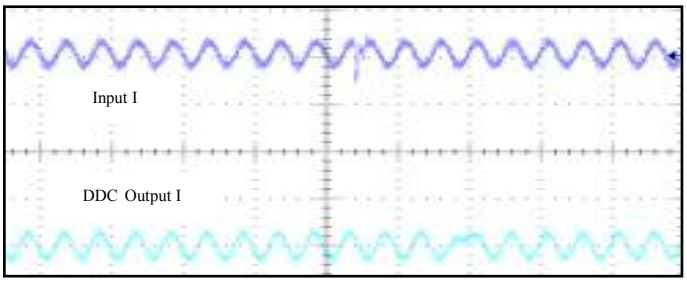

Fig. 13 : DDC I channel output

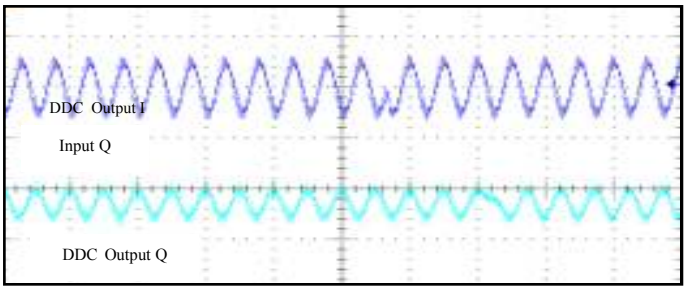

Fig. 14 :.DDC Q channel output

Compilation report of the design is shown in Table 1
Table 1

	Used Resources	Available Resources	Utilization (%)
Combinational ALUT	12369	113600	11
Memory ALUT	105	56800	<1
Dedicated Logic register	14458	113600	13
Total pins	59	744	8
Total block memory bits	5376	5630976	<1
DSP block 18 bit	12	384	3

V. Conclusion

Digital up conversion design using three stage CIC filter using multiplier based NCO have been synthesized on Stratix-III FPGA board. CIC decimator and interpolator structures are optimized in terms of hardware required for their implementation. System is designed using real time BPSK modulated signal which has low bit rate modulating data, 250kbps. Input sampling frequency of BPSK signal has 80 MHZ where final DUC output has sampling of 240MHZ. More optimized result is obtained without use of filter after the modulation which saves the resources. The 5MHZ baseband BPSK signal is brought out to an IF of 65MHZ. It has been seen from the spectrum result that the lower sideband up to 27db down then the higher sideband with carrier suppressed.

VI. Acknowledgment

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