ISSN : 2394-2975 (Online)
ISSN : 2394-6814 (Print)
Vol. 2, Issue 4 (Oct. - Dec. 2015)
International Journal of Advanced Research in Education & Technology (IJARET)

Design of Low Power 6T SRAM 8*8 Array Using Gateway Transistor

[I]Sajitha Banu.S, [II]Yogesh.R, [III]Kamalam.S
[I,II]Student of NPR College of Engineering and Technology,
NPR College of Engineering and Technology, Dindigul,Tamil Nadu.
[III]Faculty of NPR College of Engineering and Technology,
NPR College of Engineering and Technology,
Dindigul,Tamil Nadu.

Abstract
*In the modern SOC technology, there is a need of more no of transistors to store data than the transistors needed for other operations. Hence, the power of memories is also increased.So, the low power memories are vital in future. In order to reduce the power consumption of the memories, we need to reduce the leakage power. Since, leakage power plays a major role in overall power consumption. In this paper, 6T SRAM with gateway transistors is designed and the power and delay is calculated. It is implemented for 8*8 memory array. This design is done with the TANNER Eda V13.0*

Keywords
Gateway Transistors, Low Power, SRAM.

I. Introduction

The Static Random Access Memories are read/write (R/W) memory circuits which allow to modify the data bits stored in it as well as their retrieval on request. The word static comes from the fact that as long as power is on , the stored data is retrieved. The word Random Access describes that the access time is independent of the physical location of the data stored.

In the modern VLSI technology, the static RAM has a vital role because of its large storage and low latency.But, its power dissipation have to be optimized. The leakage power is the main power dissipation. To optimize the power, gateway transistors are used in this paper.

II. Literature Review

The no of transistors used in the circuit is main concern for power optimizations. Even though four transistors is enough to design the SRAM circuit, it needs the resistive loads additionally which reduces the reliability of the circuit. The writing stability of the load less 4T SRAM cell is not good [1].

To improve the writing stability the 5T SRAM cell is designed [2]. This circuit possesses the large amount of leakage power due its feedback connection.

To avoid the instability of the write operation, look ahead bias that controls the threshold voltage dynamically. This circuit uses the 7 transistors [3].

In order to reduce the leakage current, the self-controllable voltage circuit is employed. But, its data retention and transistor sizing is complicated [4].

The MTCMOS technique is more efficient than the self-controllable voltage circuit. MTCMOS is the Multi Threshold CMOS technique is used in 12T SRAM circuit [5]. In this paper, the circuit complexity is high.

To optimize the power the memristor is used. Being an analog element the memristor possesses an accountable leakage power. The overall area of the circuit is increased due to the presence of memristor [6].

III. Proposed Scheme

A. 6T SRAM

There is word line and bit line which controls the transistors. Connection to the 1-bit SRAM cell is implemented by two complementary bit lines in order to maintain the read/write margins. When the word line is not selected (WL=0) pass transistors M5 and M6 are turned off preventing the modification of the cell value, which is persevered by the latch consisting of the two cross coupled inverters. At this point, the bit lines are charged up by column pull up transistors.

If the memory cell is selected by raising the voltage of the word line to “1”, pass transistors M5 and M6 are turned on. Once the SRAM cell is selected either a read or write operation can be performed. To store logic “1” to the cell, bit line (BL’) is forced to logic “0” by the data write circuitry. This actin turns driver transistor M3 off and transistor M4 on forcing Q to logic “1”. When logic “1” is stored in the cell and the cell is selected in order to read its value, the voltage of column (BL’) is slightly pulled down by transistors M1 and M5. This small voltage difference at the bit line is sensed by the data read circuitry and amplified as logic “1” to the output. Writing and reading logic “0” is performed in the symmetrical manner.

B. 6T SRAM with Gateway Transistor

One of the methods at circuit level to reduce the leakage power is by adding two sleep transistors in 6T SRAM circuit. In the active mode, PMOS M7 gate input (S’) is kept low and NMOS M8 gate input (S) is kept high. So, both the sleep transistors are turned ‘ON’. So, according to the pass transistors property, source nodes of two PMOS SRAM load transistors are at V dd.

ISSN : 2394-2975 (Online)
ISSN : 2394-6814 (Print)

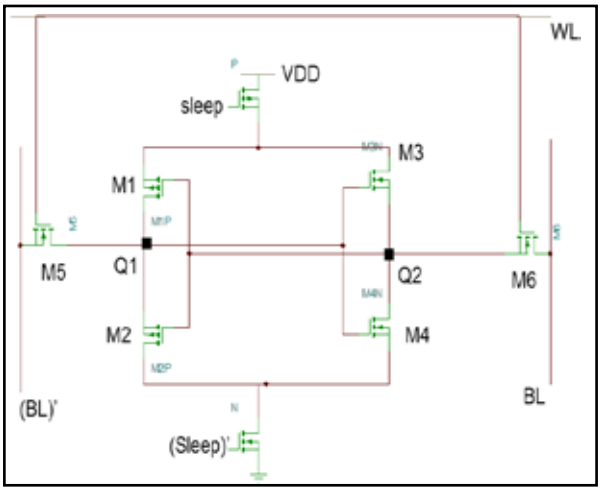

Fig. 1 : 6T SRAM with gateway transistors

C. 8*8 Memory Array Implementation

This 8*8 bit architeture have 8rows and 8 columns. It stores 64 bit data.There are 64 6T SRAM cells.

1. Address selection process

The address selection process is to identify the correct data in overall memory array cell function, then to select the read data process using the 3:8 decoding architecture design. This design is to implement the SRAM memory array architecture and to enhance the read performance level in overall SRAM memory design. The decoder architecture is to consist of basic logical gate structure and to apply the input bit in decoder architecture. Then to activate the readline bit.

2. Read bit line function

This type of address decoding sensing scheme reads the stored data very fast and it consist of combination of RBL cell. This function is to improve the read performance level and to reduce the overall leakage power consumption level. Then the stored data must be read in the read bit line (RBL).in this SRAM we can write a data in to the memory and also read that data.

IV. Simulation and Results

The 6T SRAM with gateway transistor and 8*8 memory array is designed and simulated by TANNER Eda V13.0

A. 6T SRAM CELL

1. Design

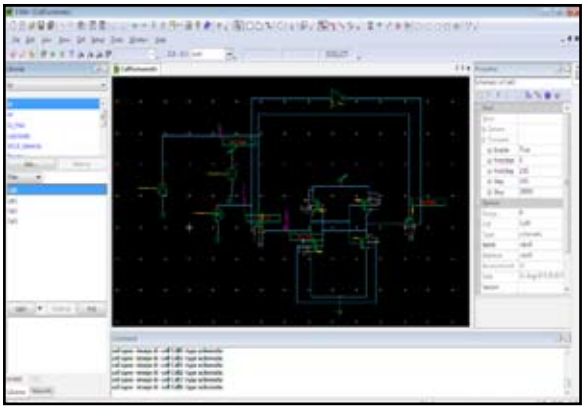
Fig. 2 : Design of 6T SRAM cell

2. Simulation

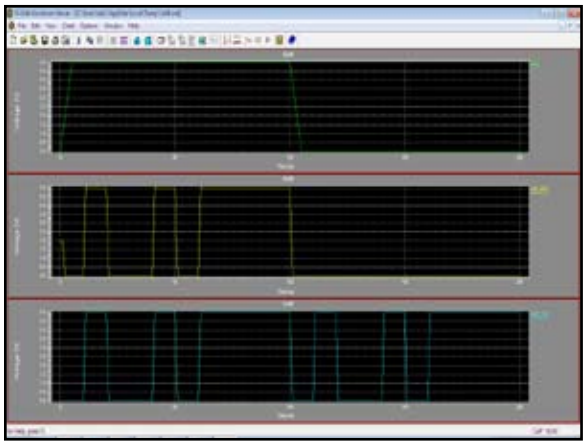
Fig. 3 : Simulation of 6T SRAM cell

3. Power

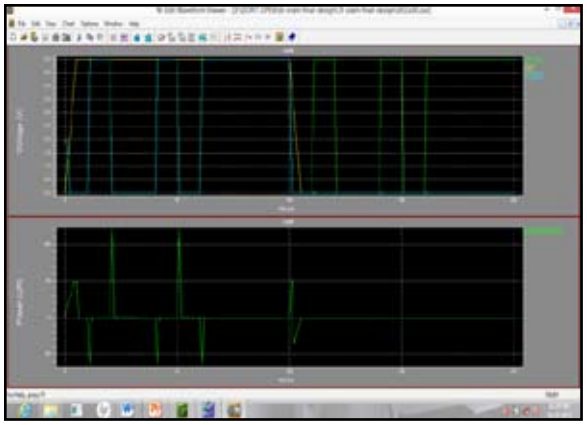
Fig. 4 : Power of 6T SRAM cell

B. 6T with Gateway Transistor

1. Design

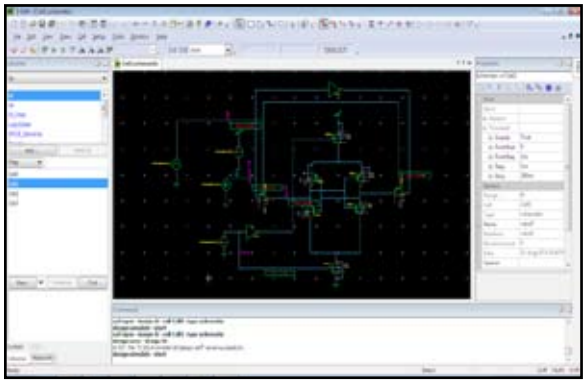
Fig. 5 : Design of 6T SRAM with Gateway transistor

2. Simulation

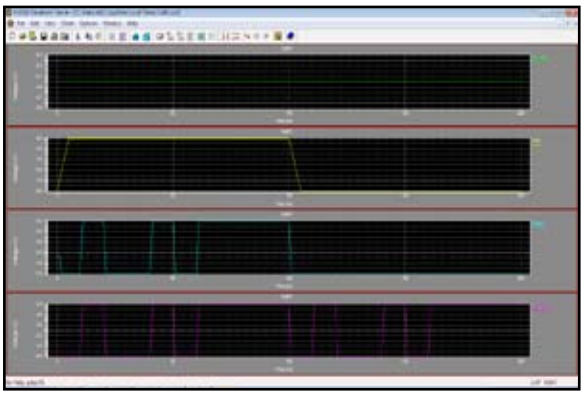

Fig. 6 : Simulation of 6T SRAM with gateway transistor

3. Power

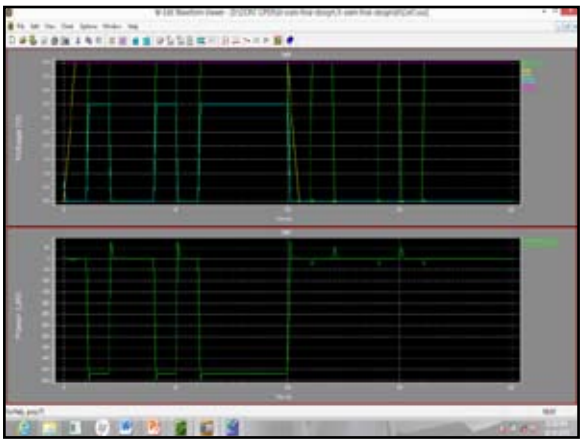

Fig. 7 : Power of 6T SRAM with gateway transistor

C. 8*8 Implementation

1. Design

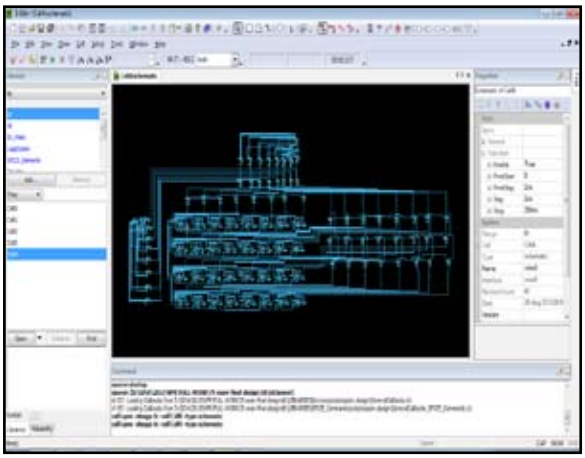

Fig. 8 : Design of 8*8 SRAM array

2. Power

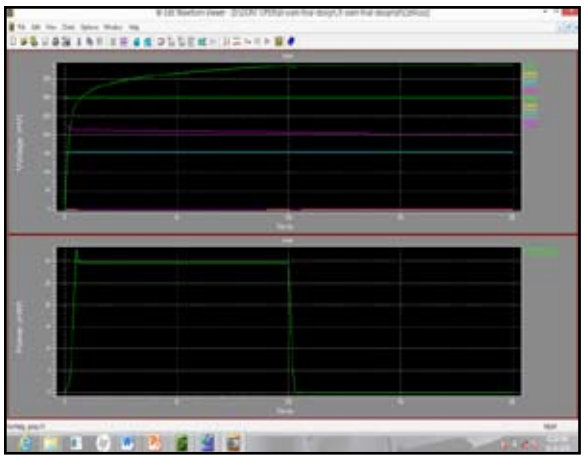

Fig. 9 : Power of 8*8 SRAM array

D. Power Comparison of Different Architectures

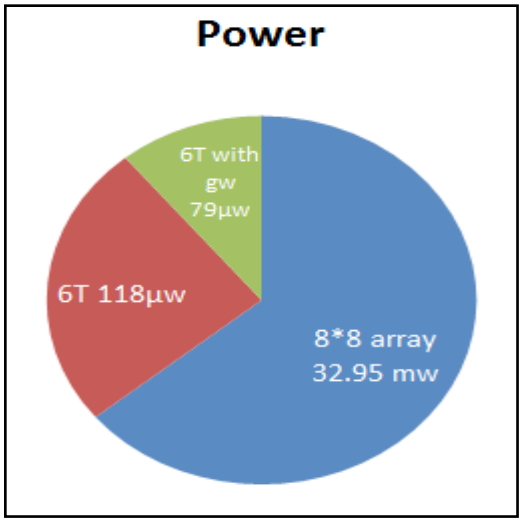

Fig. 9 : Power Comparison of Different Architectures

V. Conclusion

6T SRAM with sleep transistor technique is the best technique.It yields more power reduction. The sleep circuits reduce leakage power when these operate in "stand-by mode" due to inefficient passing of the voltages (pass-transistors property). In this system the overall transistor count is reduced.hence the area is also reduced. The 6T SRAM is designed and simulated using TANNER Eda 13.0

References

[1]. *ShyamAkashe, MayankShasthri , "Read write stability with leakage minimization of 4T SRAM cell for nano CMOS technology," IEEE Nano Science engineering and Technology,pp.355-359,2011*

[2]. *Gupta.R, Gill.S.S, Kaur.N, "A novel low leakage and high density 5T CMOS SRAM cell in 45nm technology," IEEE Conference on Recent Advances in Engineering and Computational Sciences, 2014.*

[3]. *ShyamAkashe and Sanjay Sharma," Look ahead dynamic threshold voltage control for enhanced write margin of 45 NM 7T-SRAM cell,"International Journal of the Physical Sciences Vol. 6(11), pp. 2613-2617, 4 June, 2011.*

[4]. *ShyamAkashe, Deepak Kumar Sinha and Sanjay Sharma, "A*

low-leakage current power 45-nm CMOS SRAM ,"Indian Journal of Science and Technology Vol. 4 No. 4, pp.440-442, April 2011

[5]. Upadhyay.P, Agarwal.N, Kar.R and Mandal.D, "Power and Stability analysis of proposed 12T MTCMOS SRAM cell for low power devices," IEEE Conference on Advanced Computing and Communication Technologies, 2014.

[6]. ShyamAkashe,Vijay Singh Baghel, "Low power memristor based 7T SRAM using MTCMOS technique," International Conference on Advanced Computing and Communication Technologies,2015.

Author Profile

Sajitha Banu.S was born in Tamil Nadu, India 1993.She received her UG degree in electronics and communication engineering from ANNA University, Tamil Nadu, India. She is doing her ME VLSI Design in ANNA university. Her current research interests include Low power VLSI Design.

Yogesh.R was born in Tamil Nadu, India 1991.He received his UG degree in electronics and communication engineering from ANNA University, Tamil Nadu, India. He is doing his ME VLSI Design in ANNA university. His current research interests include Low power VLSI Design.

Kamalam.S was born in Tamil Nadu,India 1972. She received her AMIE from The institutions of engineers, India. She received her PG degree in Embedded System Technologies from ANNA University,Chennai.
She is currently an Assistant Professor with NPR college of engineering and Technology, Tamil Nadu. Her current research interests include low power VLSI Design.