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VLSI Architecture For Photo Core Transform Using Parallel Multiplier in JPEG XR

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Abstract
Many advanced multimedia applications require image compression technology with higher compression ratio and better visual quality. High quality, high compression rates of digital image and low computational cost are important factors in many areas of consumer electronics, ranging from digital photography to the consumer display equipment applications such as digital still camera and digital frame. These requirements usually involve computationally intensive algorithms imposing trade-offs between quality, computational resources and throughput. For high quality of digital image applications, the extended range of color range has becoming more important in recent emerging need of the consumer product. JPEG XR is an emerging image coding standard, based on HD Photo developed by Microsoft technology. It supports high compression performance twice as high as the de facto image coding system, namely JPEG, and also has an advantage over JPEG 2000 in terms of computational cost. JPEG XR is expected to be widespread for many devices including embedded systems in the near future. In JPEG XR image compression technique the unified photo core transform is used. It is designed to support high dynamic range and high definition formats thus this type of JPEG XR image compression with unified photo core transform is widely used in real time embedded applications. In this the parallel multiplier based photo core transform is used to lower the circuit complexity and power. In this our work is to design a photo core transform. Thus this photo core transform is implemented with adder, shifter and parallel multiplier circuits by using this area cost and power consumption is reduced.

Keywords
Photo Core Transform, low power, Multiplier.

I. Introduction

To satisfy the high quality image compression requirement, the new JPEG XR compression standard is introduced. The analysis and architecture design with VLSI architecture of JPEG XR encoders are proposed in this paper which can encode 4:4:4 192 0 x 1080 high definition photo in smooth. According to the simulation results, the throughput of the proposed design can encode 44.2 M samples/ sec. This design can be used for digital photography applications to achieve low computation, lo w storage, and high dynamical range features. Many advanced multimedia applications require image compression technology with higher compression ratio and better visual quality. High quality, high compression rates of digital image and low computational cost are important factors in many areas of consumer electronics, ranging from digital photography to the consumer display equipment applications such as digital still camera and digital frame. These requirements usually involve computationally intensive algorithms imposing trade-offs between quality, computational resources and throughput. For high quality of digital image applications, the extended range of colour range has becoming more important in recent emerging need of the consumer product.

II. Literature Review

The operating frequency of the architecture is reduced by the folding transformation and register minimization techniques [1].but the delay is increased.

To reduce the delay and power consumption, the Radix-2 Decimation-In-time (DIT) architecture with carry select adder is employed[2]. The throughput is reduced due to this technique.

The time delay could be reduced by the eight data-path pipelined approach.[3]. But, the circuit complexity is increased.

To reduce the system internal complexity, Radix-25 algorithm for 512 point Fourier Transform is used.[4]. This transform consumes more power.

The multipath delay communicator (MDC) based architecture is used to improve the throughput of the architecture. Yet the power consumption of the architecture is high[5].

III.Proposed Scheme

Proposed system is a design of photo core transform usedin JPEG XR image compression. Thus this photo core transform is implemented with parallel multiplier, adder, and shifter.Thus this proposed system is designed to work in low power and the cost of this system is also low and the circuit complexity is reduced.First of all, colour space transformation is applied to an input image to transform RGB image to YUV image.

A. Transforms Functions

A transform called photo core transform (PCT) is applied to decompose an image into frequency components. The PCT is applied to a rectangular area called a macro block. To reduce block noise, this occurs around macro block boundaries, a transform called photo overlap transform (POT) is used with the PCT. Next, the transformed coefficients are quantized. In an inter-block coefficient prediction, an adaptive scanning is processed and coefficients are rearranged from two-dimension form to one dimensional form. Finally, the scanned coefficients are entropy coded using adaptive Huffman tables. Hereafter, the details of each process are described. These features make JPEG XR more flexible and suitable for hardware implementation especially when memory size constraint is in high priority. The compression ratio decreases when number of tile increases. The reason why we transform spatial data into frequency domain is: Human eyes are usually less sensitive to high frequency component so that it could be removed to reduce overhead. Frequency transform could extract frequency components which are uniformly distributed in spatial data and put same frequency components together. Once the high frequency component has been put together, it is easy to

remove them by using quantization. That is why the quantization parameters in high frequency band are usually much larger than the low frequency and DC bands. The frequency transform function used in JPEG XR is called Photo Core Transform (PCT).

B. Performances of Jpeg XR

After pre-filtering, it transforms an image from spatial domain into frequency domain, like the old Discrete Cosine Transform (DCT) from JPEG does. Adaptive prediction is used in JPEG XR. The prediction performs only when the system makes sure two neighbour macro blocks have big enough similarity. It is called "adaptive" because it dynamically changes they predict direction to one of the neighbour macro blocks which has the biggest similarity with the current macro block. The predict direction could be from left, top or top-left and the prediction scheme is variant across different frequency bands. The detailed DC, LP and HP prediction will be introduced in the following sections. DC Prediction: The DC prediction is done in between macro blocks. It can happen from top, left and top-left. The DC level of the one deemed most similar is selected and the difference between that one and the present one is calculated. The JPEG committee carried out a number of experiments to thoroughly assess the performance of JPEG XR when compared to JPEG and JPEG 2000. The coding schemes have been analysed test image data sets were selected for these experiments, representative of a variety of content relevant to today's digital photography. These high resolution images cover a broad gamut of content with distinct characteristics.

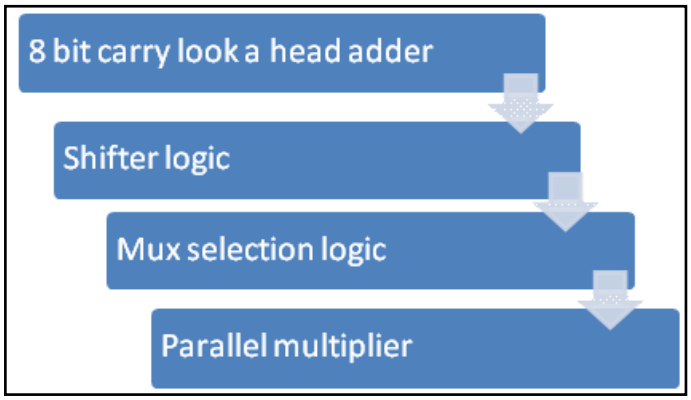

Fig.1 : System Architecture

1. Carry look ahead adder

The carry look ahead adder performs the speed and fast addition of input bit and produces the output.The carry look ahead adder circuit implemented using the full adder circuit each full adder performs single bit addition.Carry is set for first full adder then the second adder carry generated is given carry input to the next adder like this the carry look ahead adder performs the fast addition operation.Then the carry look ahead adder performs the fast addition and produces the output.

2. Shifter Logic

Shifter logic circuit is used to shift the sequence of incoming input bits.In this proposed system the right shifting logic is used to shift the incoming input bits.Thus the output of carry look ahead adder is given as input to this shifter logic then the bit is right shifted.

3. Mux Selection Logic

In the proposed system the mux selection logic is used to select the required input signal as in the output.Then thus it is also used as the switching logic. Using this output of adder circuit and the output of shifter is selected in the output of mux.Then thus the in the output of the mux logic.required output is selected.

4. Parallel Multiplier

The parallel multiplier is used to multiply the output bits of mux selection logic.In this parallel multiplier the PPG unit area is reduced thus the operation will be fast.

IV. Simulation and Results

In our proposed work we are implemented 8-bit and 16-bit adder circuit,8-bit and 16-bit shifter circuit, and parallel multiplier circuit. Thus the parallel multiplier increases the speed of the system because thus it reduces the area of the PPG unit. Thus this type of photo core transform is used to achieve the low power and very fast transformation.We can make this process through VHDL language in Xilinx 14.2 software.

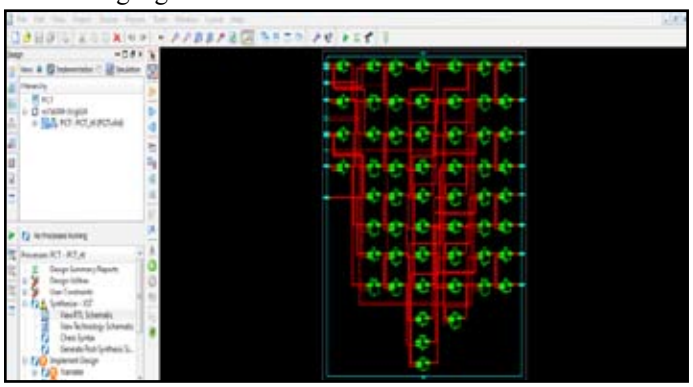

Fig. 2 : Schematic Logic

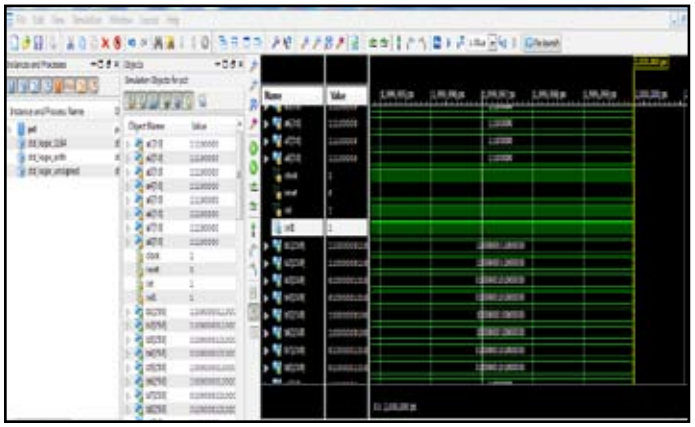

Fig.3 : Simulation Result

Fig.4 : Device Utilization

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V. Conclusion

Finally we designed a photo core transform used in JPEG XR thus this photo core transform is implemented using parallel multiplier, adder and shifter circuit thus this design reduces the power consumption.

References

[1] *Dufaux, F., Sullivan, G.J., and Ebrahimi, T.: 'The JPEG XR imagecoding standard [standards in a nutshell] ', IEEE Signal Process. Mag.,2009, 26, (6), pp. 195 –199, 204-204, doi: 10.1109/MSP.2009.934187*

[2] *ISO/IEC 29199-2: 'Information technology – JPEG XR image codingsystem--Part 2: Image coding specification', 2012*

[3] *Perra, C.: 'Re-encoding JPEG images for smart phone applications'.Proc. IEEE 21st Telecommunications Forum, Belgrade, Yugoslavia,November 2013, pp. 955 –958, doi: 10.1109/TELFOR.2013.6716389*

[4] *Pan, C.H., Chien, C.Y., Chao, W.M., Huang, S.C., and Chen,L.G.:'Architecture design of full HD JPEG XR encoder for digital photography applications', IEEE Trans. Consum. Electron., 2008, 54, (3),pp. 963 –971, doi: 10.1109/TCE.2008.4637574*

[5] *Maalouf, A., and Larabi, M.C.: 'Low-complexity enhanced lapped transform for image coding in JPEG XR/HD Photo'. 16th IEEE Int. Conf. onImage Processing, Cairo, Egypt, November 2009, pp. 5 –8, doi: 10.1109/ICIP.2009.541393.*

[6] *Tu, C.J., Srinivasan, S., Sullivan, G.J., Regunathan, S., and Malvar,H.S.:'Low-complexity hierarchical lapped transform for lossy-to-losslessimage coding in JPEGXR/HD photo'.*

Author Profile

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