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Power Analysis and Validation of Digital Circuits Based on FPGA

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Abstract

This paper proposes a model for estimation of total power and area of circuits implemented using FPGA's. The family of FPGA being used is Spartan 3. Estimation done by these models helps digital circuit targeted FPGA's, to design well-organized in terms of area, power and speed. This will be helpful for system level designer to provide reasonably correct hardware-related power estimates to guide the algorithm design process.Proposed model is designed in MATLAB by using curve fitting or regression analysis. To develop the model, synthesis ofdifferent configurations of multiplier circuits is done using FPGA's which are from Spartan 3 family. Different power standards and number of slices calculated from these different configurations has been used in curve fitting and regression analysis to design the model. Error is minimized to less than 10% for the proposed model..

Keywords

FPGA, power dissipation, power, clock gating, IP core, regression analysis, design space exploration

I. Introduction

In spite of the proceeded with lessening in power supply voltage, power dissipation will keep on increasing as the operating frequencies. In the event that the power dissipation of a circuitis high, the cost increments. The chip may require unique packaging [1]. The PCB cost additionally increments since the chip may require heat sinks or a fan and so on [2]. The space required on the Board likewise increments. If it is a portable hardware then the battery life decreases. So it is ideal to bring down power dissipation [3]. So other than logic and timing enhancement, now a day's power enhancement is likewise utilized in configuration stream of advanced frameworks [4]. The power optimization can be utilized at any phase of design cycle. At building level, more complex systems are there, which gives more extension to reduction in power. Unquestionably, this decrease in power accomplished because of timing, area, or testability of the design. Voltage, power dissipation and frequency are connected parameters.

$P = C.V^2.F$

From the above equation it is clear that whenever there is a transition, power is dissipated. The power optimization technique applied here is clock gating.

FPGA architectures can be reconfigured according to the parameters specified by the users. High performance can be achieved at low cost. The recent FPGAs have upto 500 MHz clock frequency and millions of gates, fast I/O interface and bigger on-chip memory. As a result they are an easy and cost effective way of implementation. However, the developers still prefer use the languages like C or MATLAB to validate and test their algorithms. One way of filling the gap is to use an easy method for translating the high level algorithm description onto an FPGA platform by using the parameterizable Intellectual Property (IP) cores [5]-[15]. When IP core based designed are used, it reduces the time and effort for a hardware development.

In this work certain IP corebased design like a multiplier are used. These multiplier circuits are designed using VHDL and the power is analysed using Xilinx tool. Different readings of power are noted from the XPower analyser in Xilinx. These readings of power and some other parameter are used to form an equation using curve fitting and regression analysis in MATLAB. These equation are then used in MATLAB to calculate the total power and hence validate the results with that of XPower analyser results. By comparing and validating these results, estimated error can be found.

II. Work Flow

The proposed work is a model for estimation of total power and area of circuits implemented using FPGA's for Spartan 3 family. Estimation done by these models helps digital circuit targeted FPGA's, to design well-organized in terms of area, power and speed. This will be helpful for system level designer to provide reasonably correct hardware-related power estimates to guide the algorithm design process.

The work flow for the proposed work says that it will start with the choice of digital circuits to be analyzed in the XPower analyzer. The decided circuits will be then designed in VHDL .The power of these circuits designed in VHDL will now be analyzed in XPower analyzer.

The result of XPower analyzer is stored for future reference. Then with the resources of FPGA i.e. slices, CLBs etc., an algorithm will be formed on the existing mathematical models in MATLAB.

The power calculated with these mathematical models and the XPower analyzer willbe compared and thus the error will be minimized. The block by block workflow of the proposed work is defined here in which each block shows the stepwise function of the proposed work.

The procedure of calculating the power of the digital circuits in the XPower analyzer is to choose a benchmark circuit in the FPGA. For that, first of all an FPGA family is chosen.

In this case it is Spartan 3 and under this family there are many packages, one of which can be chosen for this work which is suitable to provide the base paper level of power in mW. Fig. 1 illustrates the workflow of the proposed work where each block shows the stepwise function of the proposed work.

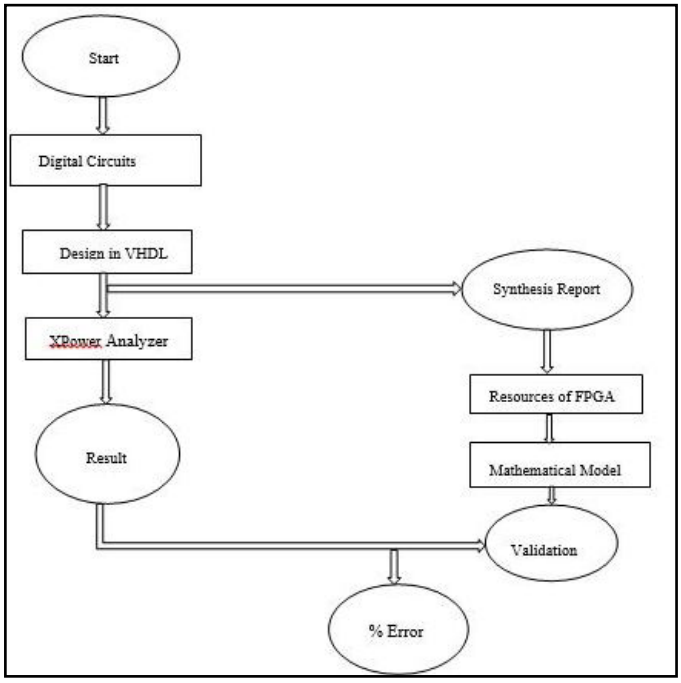

Fig. 1: Work Flow

III. ISIM Results And RTL Schematic of 64×64 Multiplier

Clock gating is a popular technique used in many synchronous circuits for reducing dynamic power dissipation. Clock gating saves power by adding more logic to a circuit to prune the clock tree. Pruning the clock disables portions of the circuitry so that the flip-flops in them do not have to switch states. Switching states consumes power.

When not being switched, the switching power consumption goes to zero, and only leakage currents are incurred. Clock gating works by taking the enable conditions attached to registers, and uses them to gate the clocks. Therefore, it is imperative that a design must contain these enable conditions in order to use and benefit from clock gating. This clock gating process can also save significant die area as well as power, since it removes large numbers of muxes and replaces them with clock gating logic

(a) Without Clock Gtaing

First of all a VHDL code is generated by choosing the type of FPGA, number of I/O ports, clock used or not and other factors. The vector length is then chosen in the benchmark circuit parameters, 64×64 in this case. Clock signal 'ce' is disabled by making it a comment in the code. This code is then synthesized and power is analysed using inbuilt XPower analyser. To simulate the behavioural model, a test bench is generated and using ISim simulator it is simulated to give a timing diagram. RTL Schematic can also be obtained which is a view of the arrangement of the circuit. Fig. 2 shows the ISim result of 64×64 Multiplier without clock gating

Fig. 2: ISim result of 64×64 Multiplier without clock gating.

Fig 3 shows the RTL schematic of 64×64 multiplier without clock gating.

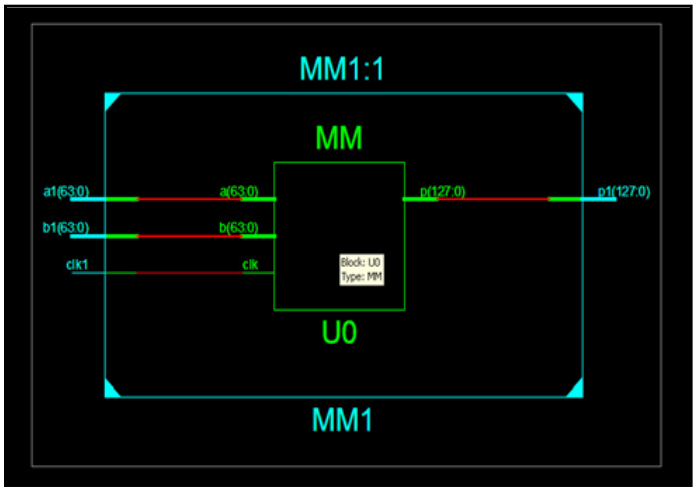

Fig 3: RTL schematic of 64×64 multiplier without clock gating

(b) With Clock Gtaing

When clock gating is applied the power dissipation is reduced to some extent. In the case of 64×64 Multiplier without the clock gating the power analyzed is 1115 mW and with clock gating it is analyzed as 1111mW. So it is visible that power is optimized. Fig. 4 and Fig.5 shows ISim results and RTL Schematicof 64×64 Multiplier with clock gating respectively.

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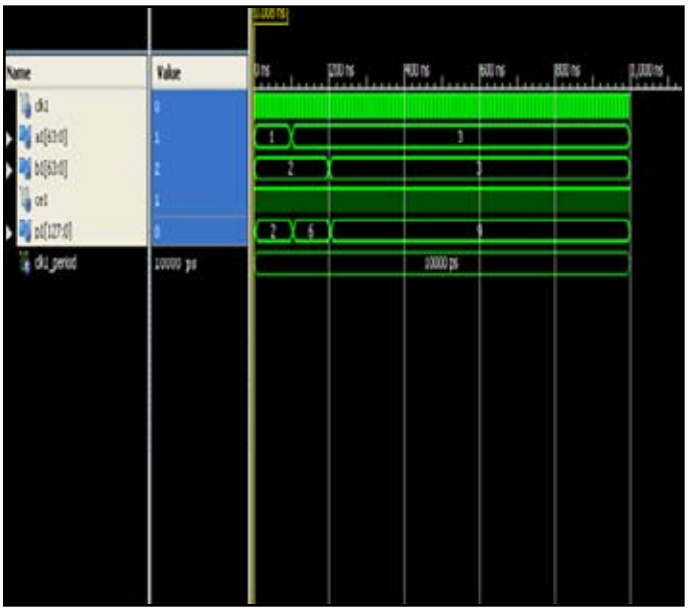

Fig. 4: ISim result of 64×64 Multiplier with clock gating.

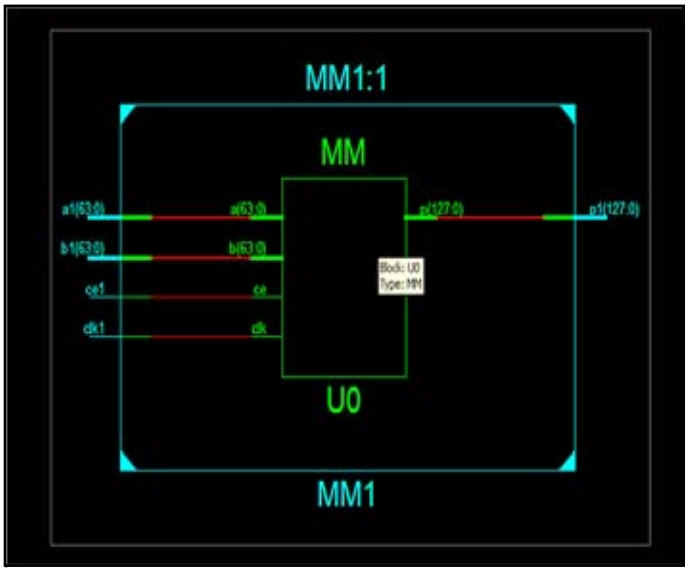

Fig 5: RTL schematic of 64×64 multiplier with clock gating

IV. Simulated Results and Validation

(a) Simulated Result of XPower analyser

Multipliers of different vector lengths are analysed in XPower analyser and their power is estimated without applying the clock gating technique of power optimization. The same multipliers are analysed again in XPower analyser but now with the power optimization technique called clock gating. We can see that the values of power dissipation are considerably reduced when clock gating technique. Fig. 6 shows graphical representation of results of XPower analyser without clock gating and with clock gating.

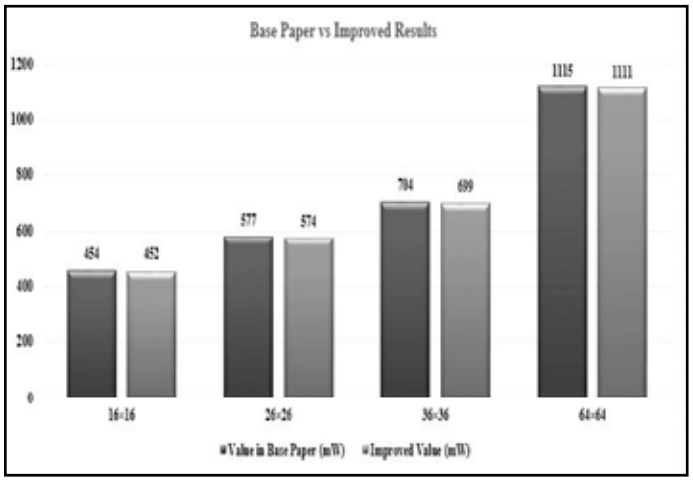

Fig. 6:XPower analyser results without clock gating and with clock gating.

And below is the tabular form of this

Table 1: XPower analyser without clock gating and with clock gating.

Multiplier design with different vector lengths	Value of Power Dissipation in Base Paper[1]	Proposed Value of Power Dissipation	Improved Value of Power Dissipation
16×16	451mW	453-450 mW	452 mW
26×26	577 mW	576-572 mW	574 mW
36×36	704 mW	703-697 mW	699 mW
64×64	1115 mW	1114-1110 mW	1111mW

(b) Simulated result of MATLAB

A synthesis report is formed from the results of XPower analyser and the data from this synthesis report is moulded into equations using curve fitting technique in MATLAB. These equations are used to calculate total power. The results of MATLAB synthesis are compared to the results of XPower analyser and hence validated. Estimated error is calculated with a formula

% Error = {(Synthesis value – Estimated Value) ÷ (Estimated Value)} × 100

Table 2 shows the comparision between the results of XPower analyser and power calculated in MATLAB.

Table 2: Validation Result comparison and error estimation

CIRCUIT	POWER in mW			NO.of COMPONENTS				POWERin mW				ERROR
Multiplier	Logic	Signal	Clock	No. of Slices	No. of M18	No. of I/P pins	No. of O/P pins	I/P power	O/P power	Total power	Est. Power	%Error
8×8	0	1	4	16	1	17	16	0.45	82.75	365	364.6574	0.09%
16×16	0	2	3	32	1	33	32	0.69	165.5	451	450.3367	0.15%
24×24	1	6	4	53	4	49	48	0.91	248.25	544	536.7219	1.40%
32×32	2	9	4	73	4	65	61	1.15	331	633	622.6762	1.63%
40×40	4	18	4	159	9	81	80	1.37	413.75	732	719.272	1.74%
48×48	5	23	4	182	9	97	96	1.59	496.49	823	806.1326	2.04%
56×56	8	42	4	332	16	113	112	1.83	579.24	934	913.1701	2.23%
64×64	10	51	4	387	16	129	128	2.05	661.99	1030	1005.4	2.30%

It can be seen that the % error is quite less. It is reduced to less than 10%.

V. Conclusion

Study of the internal architecture of FPGA and exploration of various blocks present in it. The work is an extensive literature survey related to low power techniques that can be applied at different hierarchy levels in the design to implement low power digital circuits. The various estimation models that are required for

validation purpose are also founded.Proposed model is designed in MATLAB by using curve fitting or regression analysis. To develop the model synthesis of different configuration of multiplier circuits using FPGA's from Spartan 3 family is to be done. Different power standards and number of slices calculated from these different configurations has been used in curve fitting and regression analysis to design the model. Error is minimized to less than 10% for the proposed model.

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Author Profile

Alka Shuklawas born in Rajouri, J&K. India. She has completed his secondary and higher secondary examination with science stream in 2005 and 2007 respectively. She has completed his schooling from Model Institute of Education and Research, Jammu, J&K.She received the B.Tech degree in Electronics & Communication Engineering, from Greater Noida Institute Of Technology, Greater Noida, U.P.She is pursuing M.Tech in Electronics & Communication Engineering from Ajay Kumar Garg Engineering College, Ghaziabad, U.P. (2014-2016). Her current interest includes power analysis of digital circuits based on FPGA.

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