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Characterization of 6T SRAM Cell DRV for ULP Applications

[I]Rahul Singh, [II]Uma Sharma

Abstract

This paper explore the characteristics of 6T SRAM Cell Data Retention Voltage (DRV). It also presents different DRV minimization techniques for Ultra low power applications. The 6T SRAM cell is designed in 32nm CMOS technology. The cell is simulated to through varying different DRV dependent specifications to understand the effects on it.

Keywords

CMOS, SNM, DRV, CR, PR.

I. Introduction

SRAM is used in VLSI systems. it is because of its built in speed. The SRAM cells are designed having transistors of minimum size, thus making it more accessible to process variations.

Stability is great concern for SRAM cell design. This stability defines how the memory is concerned by process variation & operating conditions. The objective is to operate the memory correctly even if noise is present.

The analysis of stability of SRAM cell in the presence of DC noise is compassed by Static Noise Margin (SNM). SNM is the amount of voltage noise appropriate to flip the state of the cell. It can be accessed from the voltage transfer characteristic (VTC) of the two cross coupled inverters of the SAM cell.

Figure 1 shows the schematic of a mainstream 6T SRAM cell. It consists of six transistors. Four transistors (M1−M4) contain cross-coupled CMOS inverters and two NMOS transistors M5 and m6 implement read and write access to the cell. Upon the stimulation of the word line, the access transistors connect the two internal nodes of the cell to the true bit lines (BL) and the complementary (BLB) bit lines. A 6T CMOS SRAM cell is the most attractive SRAM cell due to its admirable strength, low power and low-voltage operation. An SRAM cell must be constructed such that it provides a non-destructive read operation and a stable write operation. These two requirements impose contradicting concerned on SRAM cell transistor sizing

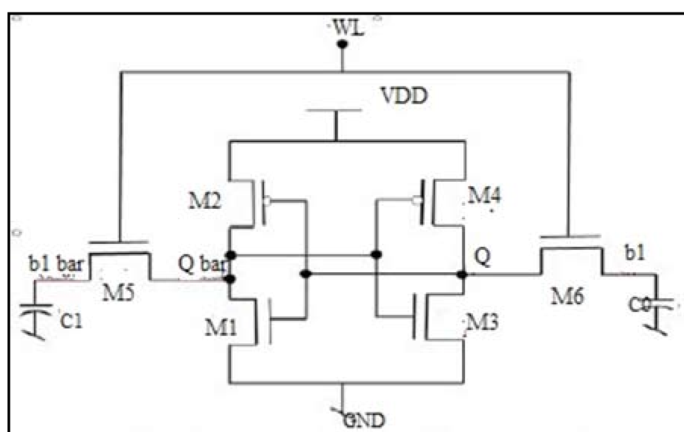

Fig. 1 : Six-transistor (6T) CMOS SRAM cell

For calculation of SNM (& indirectly DRV) method explain with the help of figure 2. It consists of two inverters coupled back to back. The sources Vn are the noise sources linked to the input and output of the two cross connected inverters . The two inverters influence the bi-stable state and their outputs nodes maintain the voltage level stored in the cell. As the noise voltages Vn increases, the output nodes voltage changes, this depict the SNM i.e. the allowed voltage levels of noise and the capability of the inverters to hold the state in the presence of noise.

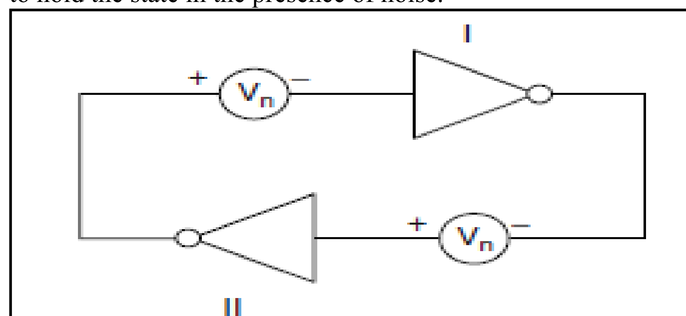

Fig. 2 : Inverters with two noise sources with adverse polarities

The SNM depends on Vth, VDD and cell ratio. So to improve the SNM performance of the SRAM cell, the cell ratio must be increased but increasing cell ratio means increasing the SRAM cell area. Thus the pull up ratio is important during write operation as its value determines how prosperous write operation can be performed under worst case conditions.

The aim of this paper is to present techniques to minimize the DRV, the parameters on which DRV is majorly dependent and the simulation results to show the effects of DRV & SNM vulnerable parameters.

II. Parameters on Which DRV is Dependent

The DRV is dependent on process and design parameters. Fluctuation in temperature & process variation causes deterioration in SRAM cell performance and imbalance between two cross coupled inverters has a strong impact on its DRV. This imbalance could be global or local i.e. variation in Vth & length of the transistors of the inverters may result in substantial change in the DRV of the cell. Other parameter is temperature fluctuation, its affects has a weak influence on DRV as the innovation in transistors properties of the inverter is uniform.

III. DRV Minimization Technique Existing & Prroposed

(a) DRV minimization using Driveability Ratio

The most popular way to improve DRV is to improve SNM performance and traditionally. it was achieved by increasing the cell ratio in other words the ratio of the driver transistor’s W/L to the access transistor’s W/L but this technique cannot be applied as the SRAM cell is also constantly scaling and it would result into increase in cell area. Another technique is decreasing driveability ratio will lead to improvement in SNM performance without cell

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area penalty.
The driveability ratio is illustrate as the ratio of the current driveability of the access and load transistors. In addition to this definition consider the same device size, the current driveability of each driver transistors is twice of each load transistor. The driveability ratio is derived for Write Noise margin (WNM) as this WNM is actually the difference of magnitude in driveability between PMOS load and NMOS access transistors in the SRAM. So the designing of SRAM cell inverters has to be done carefully previously calculating the write margin of SRAM cell during write operation. Pull up ratio also depends on the size of the transistor.
In CMOS process the NMOSFET current drive is about twice that of same width PMOSFET, this alone provides the. sufficient DC noise margin for write operation but for SNM it's unacceptable. So the WNM & SNM follow opposite trends and largest the driveability ratio is , easier way to flip the state of the two inverters during read/write operation which gives better WNM but poor SNM and it is also evident from that the impact of driveability ratio is stronger than the cell ratio on WNM.

(b) DRV minimization by variation in length & Width of SRAM Cell Transistors

As the technology scaling progresses, the need as DRV scaling with technology is a major concern. Now days ULV SRAM memories are fabricated that targets ULP systems. But with voltage scaling, comes severe reliability hazard of SRAM data storage. So in order to conformed the voltage scaling of CMOS technology and low power design requirements, the degradation of DRV must be carefully completed. So the effective technique to reduce the DRV with minimum secondary effects, area, hardware cost and performance as ULV and ULP designs, the sizing of SRAM is the solution. The sizing of access transistors has a small impact on DRV because the two access transistors doesn't significantly change the conducting path formed by the strong pull down NMOS transistor and the weak pull up PMOS device.
In a non ULV performance improve the SRAM cell, the pull down NMOS devices are sized about 2x larger than the PMOS devices. These NMOS transistors are also with minimum length to minimize cell area is also highly sensitive to process variation, which results in increase in DRV. There are certain techniques at circuit and architectural level that contribute to minimization of DRV by suppressing the leakage current in memories.

(c) DRV minimization at circuit level

At the circuit level, the efficient method of minimizing leakage power are to lower supply voltage and increase transistors threshold voltage (Vth), both degrades the speed of memory read/write operations and due to this reason it is not employ in performance critical memory design.
Another process is dynamic control of transistor gate-source and substrate-source bias to increase driving strength during read or write operation and low leakage paths during standby periods. Another technique is the negative word-line driving (NWD) design. It uses low Vth access transistors with negative cut-off gate voltage and high Vth cross-coupled inverter pair with boosted gate voltage to realize both improved access time and reduced standby leakage power. Last technique is Dynamic Leakage cut-off (DLC) scheme, in this the substrate voltages of non-selected SRAM cells biased at a voltage of ~2VDD for Vnwell and ~ -VDD for Vpwell.

(d) DRV minimization at architectural level

At architectural level, leakage reduction techniques include gating-off the supply voltage (VDD) of idle memory sections, or establish less frequently used sections into drowsy standby mode. To achieve optimal power-performance tradeoffs, compiler-level cache activity analysis are occupied to balance the potential for saving leakage energy against the loss incurred in extra cache misses. To added exploit leakage control in caches with large utilization ratio, the approach of drowsy caches appropriate inactive cache lines to a low-power mode, where VDD was lowered while preserving memory data.

IV. Simulated Result

1. Variation of supply voltage and static noise margin

SNM is a key performance factor during read & write operations. During read operation SNM takes its lowest value and the state of cell is weakest. The SNM value depends on the Cell Ratio (CR), Pull up Ratio (PR) and Supply voltage. In this section simulation results of SNM variation on different parameters is measured & shown in plots. Apart from these parameters, observation on other parameters related to process variation & temperature fluctuation are also done. In process variation, the threshold voltage of load & driver transistors is varied and its effects on SNM are observed. Similarly the effect of temperature variation above & below the room temperature on SNM is observed & calculated.
The stability of the cell is important parameter to be considered which is measured by the Static Noise Margin (SNM) of a cell. Therefore, method to calculate SNM and its effect on various parameters such as Temperature , supply voltage cell ratio pull up ratio, data retention voltage. in Table 4.1 shows the variation SNM and supply voltages whereas temperature is constant 25 ºC.

Table 4.1: Supply voltage Vs SNM

Temperature (ºC)	Supply voltage(V)	Static Noise Margin(mV)
25	1.2	218.38
25	1.1	191.59
25	1.0	165.00
25	0.9	138.58
25	0.8	112.33
25	0.7	86.486
25	0.6	66.358
25	0.5	48.266
25	0.5	30.707

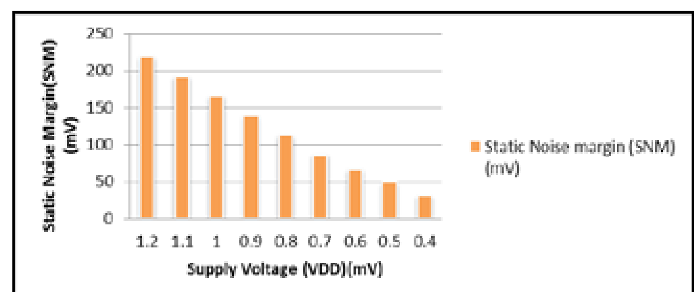

Fig. 3 : Supply voltage Vs SNM

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2. Variation of temperature and static noise margin

The stability of the cell is important parameter to be considered which is measured by the Static Noise Margin (SNM) of a cell. Therefore, method to calculate SNM and its effect on various parameters such as supply voltage, temperature,cell ratio pull up ratio, data retention voltage. in Table 4.2 shows the variation SNM and temperature whereas supply voltage is constant at 1.2.

Table 4.2: Temperature Vs SNM

Supply Voltage(Vdd)(V)	Temperatue(°C)	Static Noise Margin(mV)
1.2	10	213.79
1.2	15	215.33
1.2	20	216.86
1.2	25	218.38
1.2	30	219.89
1.2	35	221.39
1.2	40	222.88
1.2	45	224.35

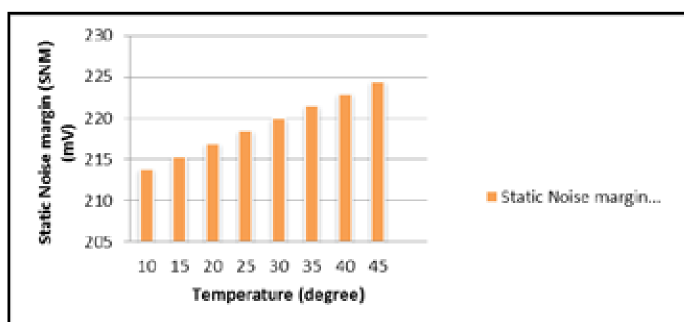

Fig. 4 : Temperature Vs SNM

3. Variation of pull up ratio and static noise margin

Table 4.3 : Pull up ratio Vs. SNM

Pull Up Transistor	Wp(n)	Static Noise Margin(mV)
1	48	197.25
2	96	222.18
3	144	234.18
4	192	242.97
5	240	248.81
6	288	253.24
7	336	256.74
8	384	259.59

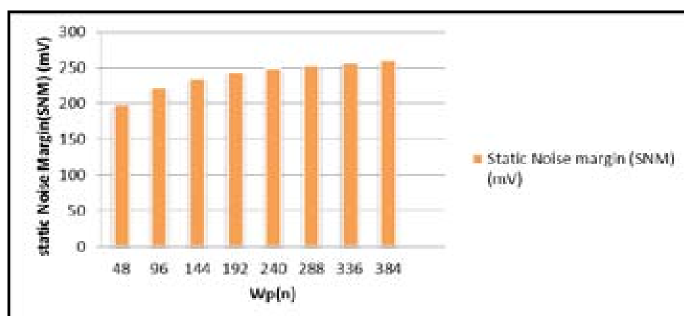

Fig. 5 : Pull up ratio Vs. SNM

4. Variation of cell ratio and static noise margin

Table 4.4 Wn Vs SNM

Pull Down Transistor	Wn(n)	Static Noise Margin(mV)
2	96	229.73
3	144	254.58
4	192	267.00
5	240	274.40
6	288	279.30
7	336	282.78
8	384	285.39
9	432	287.41

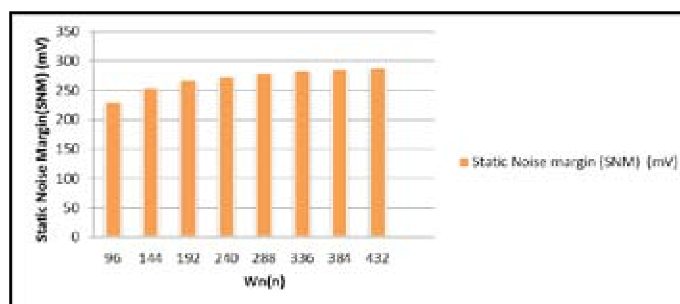

Fig. 6 : Wn Vs SNM

5. Variation of threshold voltage for NMOS and SNM

Table 4.5 : Threshold voltage for NMOS Vs SNM

Supply Voltage(Vdd) (V)	Vt,n(V)	Static Noise Margin(mV)
1.2	.15	176.75
1.2	.20	190.50
1.2	.25	204.61
1.2	.30	218.62
1.2	.35	232.38
1.2	.40	244.44
1.2	.45	256.59
1.2	.50	268.38

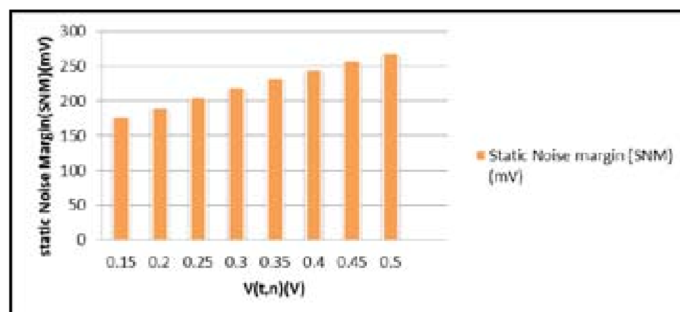

Fig. 7 : Threshold voltage for NMOS Vs SNM

6. Variation of threshold voltage for PMOS and SNM

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Table 4.5 : Threshold voltage for PMOS Vs SNM

Supply voltage (Vdd) (V)	Vt,p (V)	Static Noise Margin(mV)
1.2	-.15	131.18
1.2	-.20	155.97
1.2	-.25	179.56
1.2	-.30	201.60
1.2	-.35	221.72
1.2	-.40	239.71
1.2	-.45	255.27
1.2	-.50	268.01

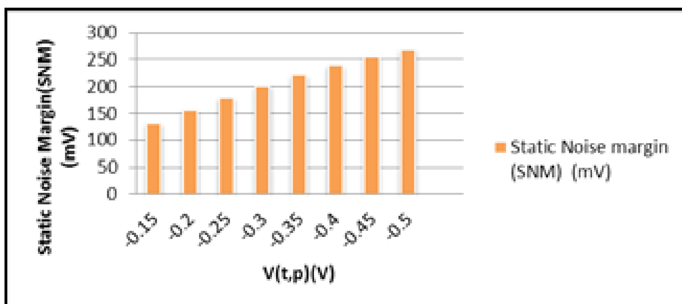

Fig. 8: Threshold voltage for PMOS Vs SNM

V. Conclusion

This paper present the limitations put on DRV under SRAM size scaling and under ULV. The DRV is concluded to be strongly dependent on process variation and also on temperature fluctuation. The DRV minimization techniques are discussed that further reduces the DRV but at the cost of SRAM cell area. This paper also present the effects of supply voltage, process variation and temperature fluctuation on SNM through simulation on 32nm CMOS technology. In addition to this effects of Cell Ratio and Pull up Ratio are also observed. The DRV minimization in this has been discussed at circuit level, the techniques comes at architectural level for achieving higher stability in ULV applications.

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Author Profile

Rahul singh was born in Ghaziabad, U.P. India. He has completed his secondary and higher secondary examination with science stream in 2006 and 2009 respectively. He has completed his schooling from National public school Ghaziabad U.P. He received the B.Tech degree in Electronics & Communication Engineering, from HR Institute Of Technology Ghaziabad, U.P. He is pursuing M.Tech in VLSI Design from Ajay Kumar Garg Engineering College, Ghaziabad, U.P. (2014-2016). His current interest 6T SRAM cell using DRV.

Uma sharma was born in Aligarh, India in 1986. He received the B.E.& M.Tech. degree in Electronics and Communication Engineering from UPTU & vanastahali, in 2008 & 2012, respectively. He started his teaching career in 2012 and is currently working as an Assistant Professor in Ajay Kumar Garg Engineering College Ghaziabad. His main areas of research interest are Analog and mixed circuit design.

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