ISSN : 2394-2975 (Online)
ISSN : 2394-6814 (Print)

Low Power Ripple Carry Adder using Pseudo Dynamic Buffer Logic

[I]Krishna M, [II]Mohan Reddy P, [III]Anita Angeline A
[I,II,III]School of Electronics Engineering, VIT University, Chennai, India.

Abstract
Power saving has become more important, with the recent rapid advancements in technology.Domino logic circuit style is one of the basic power efficient circuits due to the reduced number of transistors. The speed performance is also improved owing to the evaluation by the nmos transistors alone. This paper mainly details the design of 4 bit Ripple carry adder using Pseudo dynamic buffer logic which is a variant of dynamic logic. The simulation results are compared with the conventional domino logic in terms of power consumption, delay and leakage power. It demonstrates 39.4% reduced power consumption and increased speedof 32.2%. The simulations are performed using Cadence Virtuoso® at 180nm technology node library.

Keywords
Full adder, dynamic logic, domino logic, Pseudo dynamic buffer logic, Ripple Carry Adder

I Introduction

In this digital era, there is an enormous increase in the number of portable applications which requires low power and high performance circuits. Therefore, low-power design has become a major design challenge. Addition is a fundamental operation in every arithmetic circuit and almost all operations are based on addition. These operations are predominantly used in many VLSI applications, as the full-adder cell is the basic building block. Thus, the performance of a 1-bit full-adder is a major factor in all arithmetic circuits. Thus, improving the performance of the full adder block leads to the enhanced performance of the entire system performance. Therefore, many researchershad put-forth various methodologies to implement high-speed and low-power 1-bit full adder cells with reduced area.
A full adder cell is a multi-input multi-output system with three-inputs and two-outputs [1]. The functionality of a full adder cell is given as in Eq. (1) and Eq.(2)

$$Sum = A \oplus B \oplus Cin \quad (1)$$
$$Cout = A.B + A.Cin + B.Cin \quad (2)$$

In this paper, the design of 4 bit ripple carry adder using pseudo dynamic buffer logic is performed.

II. Dynamic Logic

Dynamic logic is an alternative logic style to static CMOS design, where N+2 transistors are only necessary in contrast with the 2N transistors used in the static CMOS design style [2]. The special features of dynamic logic circuits include: faster switching speeds, no static power consumption, non-ratioed logic, full swing voltage levels and less number of transistors [2,3]. Thestatic power consumption in dynamic circuits is reduced owing to the clock signal which enables either the PDN or the pmos pre-charge device only at a particular time. Hence, there is no static path exists between VDD and GND and eliminates the static power consumption. Thus the dynamic power is the major part of the power consumption due to the transitions at the output caused because of the precharge and evaluation phases. Since the evaluation is performed by the nmos transistors, the dynamic logic design offers high speed of operation which is a major advantage. Dynamic circuits are very useful in circuit design to attain higher speed, smaller area and potentially lower power consumption.

The clock signal dictates the operation of the dynamic logic circuit. The domino logic circuit consists of two phases. The first phase, when Clock is **LOW**(0), is called the precharge phase and in the second phase, when Clock is **HIGH** (1), is called the evaluation phase. In the initial phase, the output is driven high thoroughly (no matter what is the values of the inputs) because the transistor at the footer transistor is turned off, hence the output doesn't discharge during this phase. During the evaluation phase, the clock is high, and the footer transistor is turned ON [3]. This enables the discharging of the output dynamic node if the PDN evaluates the logic to be TRUE. However, the dynamic logic circuits when cascaded, doesn't work properly or evaluates falsely. This is due to the same clock triggering the successive stages which leads to the evaluation of the second stage even before the evaluation of the preceding stage. This is overcome by having a static inverter at the dynamic node which is referred as domino logic style. This facilitates the evaluation of the subsequent stages flawlessly.

III. Domino Logic Circuit Style

The schematic of a conventional clock controlled domino logic circuit, consists of a dynamic logic of N-type gate (Pull-down network PDN) followed by a static inverter. Fig.1 illustrates the structure of domino logic [4]. The gate operates in two phases, namely pre-charge and evaluation phases. During the pre-charge phase, while the clock signal is LOW turnsON the PMOS pre-charge transistor and makes the dynamic node to HIGH. During the evaluation phase, while the clock signal isHIGH, the footer NMOS transistor is turned ON and facilitates discharging depending upon the PDN evaluation. If the inputs are LOW, the dynamic node Z is retainedHIGH. However, when the inputs are HIGH, the dynamic node discharges and make the output LOW.

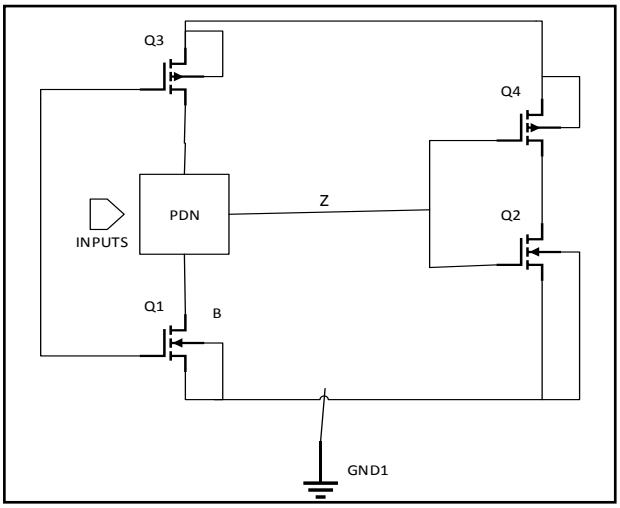

Fig 1: Conventional Domino Logic

Thus for every pre-charge phase, the output node goes HIGHand during the evaluation phase it is determined by the logical values of the input [5]. Hence, for two successive phases even if the inputs are LOW, due to the pre-charge operation, the output goes LOW in between the HIGH output during the evaluation phase. This makes the dynamic power consumption to be higher than that of the static CMOS circuits.

IV. Pseudo Dynamic Buffer based Domino Logic

To get rid of the dynamic power consumption, in the pseudo dynamic buffer logic, the previous stage output is retained during the pre-charge phase also.In the PDB-based domino logic as shown in Fig 2. the source of the nmos device M5 present in the static inverter is not grounded. Instead, it is connected to the footer transistor node B. Thus the charge at the node Z is prevented from discharging during the pre-charge phase as the evaluation transistor M2 is turned OFF [6].

In the PDB based domino logic, if the input logic A is **LOW**, the floating node Z is always **HIGH**which makes the output node F to beLOW regardless of the operating phase. Whereas if the input A is HIGH, the node Z is and node B goes LOW, and results in enabling the PMOS transistor M4, which makes the output F to attain HIGH. During the pre-charge phase, the node Z attains HIGH, and the node B is also HIGH (due to the previous evaluation). Since the NMOS evaluation transistor M2 is disabled, the output node Z is retained HIGH. This feature of disabling the discharge path due to the CLOCK LOW condition makes the PDB structure to retain the output of the previous evaluation phase during the precharge phase also. This helps in reducing the dynamic power consumption.

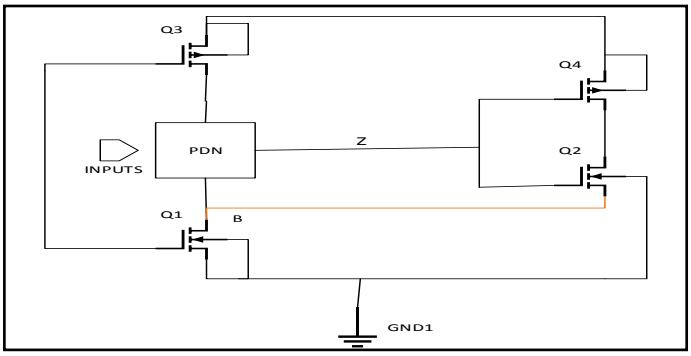

Fig 2: PDB Circuit

V. Design of Ripple Carry Adder

A ripple carry adder is a logic circuit in which the carry-out of each full adder is the carry in of the succeeding next most significant full adder. It is called a ripple carry adder because each carry bit gets rippled into the next stage [7].

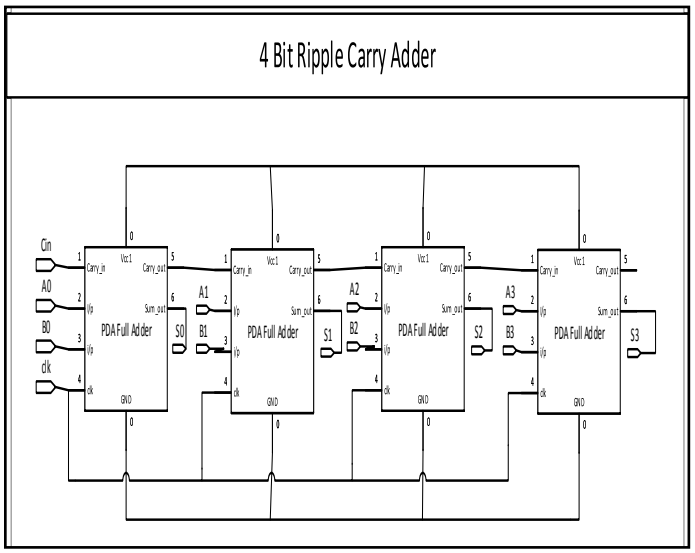

Fig 3: 4-Bit Ripple Carry Adder

A two stage cascaded adder cell is realized, where the first stage is to generate carry and the second stage is to calculate sum from carry of the first stage [6]. The expression of carry remains the same as (1) while the expression for sum is given as:

$$Sum = C_{out}^{'}(A + B + C_{in}) + A.\,B.\,C_{in} \quad (3)$$

The general block diagram for the adder implementation is given below:

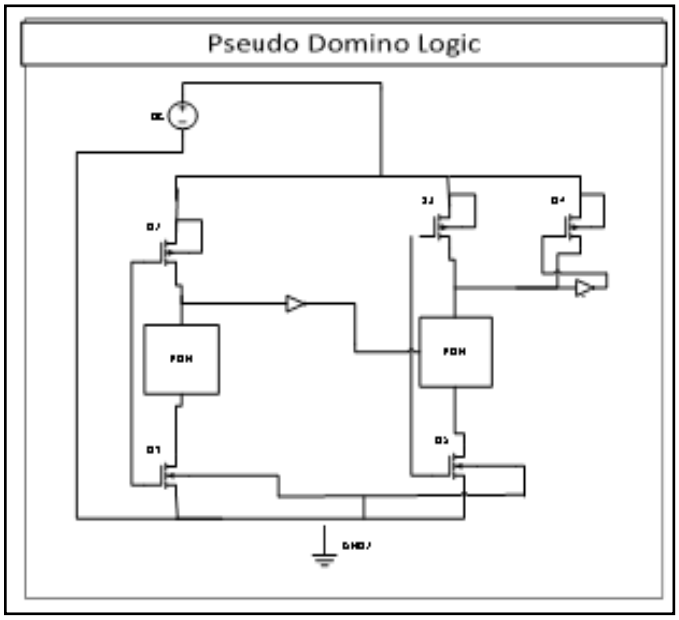

Fig 4: Full Adder Implementation

The SUM (fig.4) and CMOS (Fig. 5) CMOS dynamic logic realizations are as below:

ISSN : 2394-2975 (Online)
ISSN : 2394-6814 (Print)

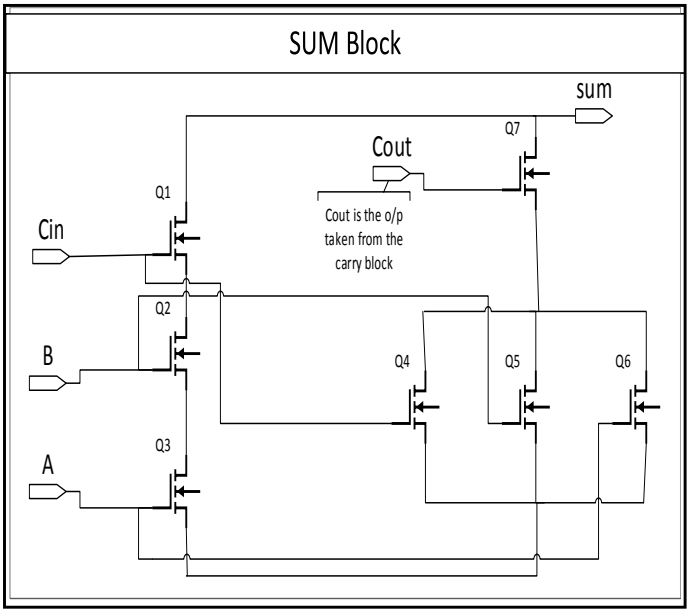

Fig 5: Sum using CMOS

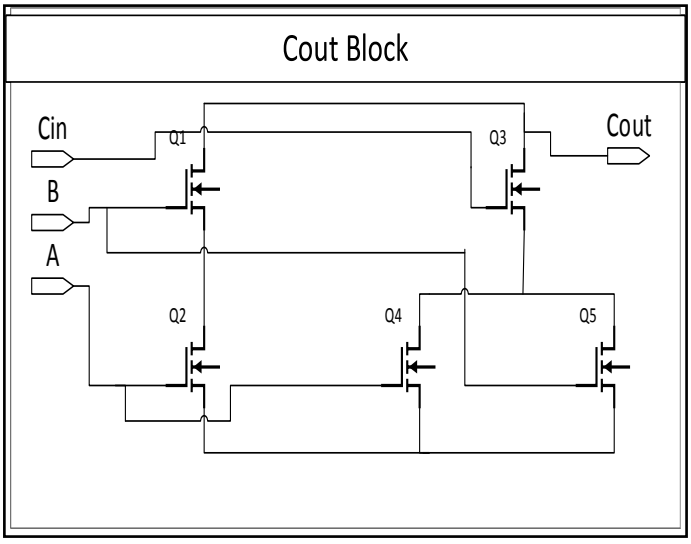

Fig 6: Carry using CMOS

These logics were implemented in the styles mentioned below and a comparative study was done.
Domino Logic
Pseudo Dynamic Buffer

VI. Simulation and Analysis

The design of ripple carry adder using conventional domino logic and pseudo dynamic buffer logic is performed using Cadence®Virtuoso at 180nm technology node. The circuits demonstratepower, propagation delay and leakage power as shown in Table 1.

Table 1 : Full Adder using Conventional domino Logic and PDB Logic

Figure of Merit	Conventional domino Logic	PDB logic
Power (W)	28.90e-6	17.50e-6
Delay (s)	46.34e-9	44.92e-9
Leakage Power (W)	611.3e-9	76.88e-12

The power and delay values for ripple carry adder are given as below:

Table 2 : Ripple Carry Adder Design

Power (W)	108.2e-6
Propagation Delay (s)	209.6e-6

VII. Conclusion

Power Saving calculated from the experimental results shows that by utilizing the pseudo dynamic buffer logic instead of domino logic 39.4% power saving is possible. There is no static power consumption in dynamic circuits. It only consumes dynamic power as there is no static path between VDD and GND. Higher speed is the major advantage of the dynamic logic design. Lower number of transistors per gate and absence of short circuit current are the reasons for faster switching speeds.

References

[1] *N. Weste and K. Eshraghian, Principles of CMOS VLSI Design: A System Perspective, Addison-Wesley, Reading, Mass, USA, 1993.*
[2] *J. P. Uyemura, Introduction to VLSI Circuits and Systems John Wiley & Sons, New York, NY, USA, 2002.*
[3] *N. Weste and D. Harris, CMOS VLSI Design, Pearson Wesley, 2005.*
[4] *U. Ko, P. T. Balsara, and W. Lee, "Low-power design techniques for high-performance CMOS adders," IEEE Transactions On Very Large Scale Integration (VLSI) Systems, vol. 3, no. 2, pp. 327–333, 1995.*
[5] *Pramod Kumar Jain, Atul Wakodkar, "Design and Simulation of Low Power Full Adder using Footed Diode Domino Logic", IJICCRE Vol. 4, Issue 7, July 2016*
[6] *Fang Tang, Amine Bermark,ZhouyeGu,"Low power dynamic Logic design using a pseudo dynamic buffer INTEGRATION", The vlsijournal45(2012) 395-404.*
[7] *S. Goel, A. Kumar, and M. A. Bayoumi, "Design of robust, energy efficient full adders for deep-sub micrometer design using hybrid-CMOS logic style," IEEE Trans. Very Large Scale Integation (VLSI) Syst., vol. 14,no. 12, pp. 1309–1321, Dec. 2006*
[8] *G.SindhuraBhargavi, T.Kalyan,"Low Power Dynamic Logic Circuit Design Using Footed Diode Domino Logic",International Journal of Engineering Research,Volume No.3 Issue No: Special 2, 22 March 2014*
[9] *A.K.Pandey, R.A. Mishra, R.K. Nagaria,Low power dynamic buffer circuit, VLSICS, VoI.3,No.5,Oct.20 12,Pg.53-65.*
[10] *R.H.Krambeck,Charles.M.Lee,"High speed compact circuit with CMOS",,IEEE Journal of Solid-State Circuits17(3):614-619*
[11] *FarshadMoradi , Tuan Vu Cao , Elena I. Vatajelu , Ali Peiravi , "Domino logic designs for high-performance and leakage-tolerant applications" INTEGRATION, the VLSI journal 46 (2013) 247–254*
[12] *S. Wairya, R. K. Nagaria, and S. Tiwari, "New design methodologies for high speed mixed mode Full Adder circuits," International Journal of VLSI and Communication Systems, vol. 2, no. 2, pp. 78–98, 2011.*
[13] *N. Zhuang and H. Wu, "A new design of the CMOS full adder," IEEE Journal of Solid-State Circuits, vol. 27, no.*

5, pp. 840–844, 1992.

[14] A. P. Chandrakasan, S. Sheng, and R. W. Brodersen, "Low-power CMOS digital design," IEEE Journal of Solid-State Circuits, vol. 27, no. 4, pp. 473–484, 1992.

[15] Yingtao Jiang Al-Sheraidah, A. Yuke Wang Sha, E. and Jin-Gyun Chung, "A novel multiplexer-based low-power full adder," IEEE Transactions on Circuits and Systems: Express Briefs, vol. 51, no. 7, pp.345-348, Jul. 2004

[16] Chip-Hong Chang, JiangminGu and Mingyan Zhang, "A review of 0.18μm full adder performances for tree structured arithmetic circuits," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol.13,no.6,pp.686-695, Jun.2005.

Author's Profile

Krishna M is pursuing his B-Tech degree in Electronics and Communication Engineering at the School of Electronics Engineering, VIT University, Chennai.

Mohan Reddy Pis pursuing his B-Tech degree in Electronics and Communication Engineering at the School of Electronics Engineering, VIT University, Chennai.

A Anita Angelinereceived her bachelor degree in the year 1999 and her Masters in Applied Electronics in the year 2004 from Karunya Institute of Technology, Coimbatore. Currently she is working as an Assistant Professor and pursuing her Ph.D degree at VIT University, Chennai. Her research areas are low power design, dynamic logic structures with process variation tolerance.