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Advanced Harmonic Elimination Techniques analysis for Various Neutral-Point-Clamped Inverters Fed Induction Motor Drives

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Abstract

This paper proposes that to elimination of unconditional harmonics and common mode voltage reduction in inverter fed induction motor drives. Here we introduce the scheme of SHEPWM, which includes C-SHEPWM and M-SHEPWM. By using C-SHEPWM scheme the modulation index increases up to 1.15,which is used to control the inverter fed induction motor at high frequencies. In M-SHEPWM scheme the modulation index decreases up to 1,which is used to control the inverter fed induction motor drive at low frequencies. This method is high efficient in common mode voltage reduction compare with passive filter by using neutral point clamped inverter fed method. As the simulation result shows that the proposed SHEPWM technique ,which eliminate the harmonics and reduce the common mode voltage. The required modulation index can also be achieved in this method.

I. Introduction

Multilevel inverter is used to synthesize the desired AC from several levels of DC. As the number of levels increases the harmonic content decreases. Here the multilevel inverter used is the Neutral-point-clamped (NPC) inverters.NPC is used to drive medium-voltage high-power ac motors because of their high-voltage and high-power capacity and efficient harmonic performance. Such motor drives are used in many applications, such as high-power pumps and fans, leading to high energy savings .

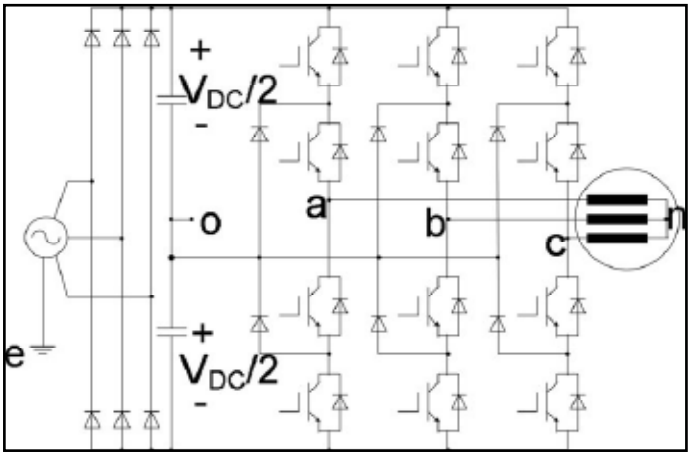

Fig.1 : Three Level Neutral point NPC fed IM drive

Even though it has many advantages, similar to two-level inverters, different NPC inverters generate common-mode voltage (CMV). The CMV in a three-level NPC inverter fed induction motor drive is shown in Fig. 1. The CMV is defined as the voltage between the neutral point of the motor (node *n)* and the earth ground (node e), i.e., V_{ne}. V_{ne} have two component voltages: one is the voltage from the neutral point of the motor to the mid-point of the dc link, i.e., V_{no} and the other is the voltage from the mid-point of the dc link to the earth ground, i.e, $V_{oe.}$ The three level and five level circuit diagram is similar, the only difference in the number of the switching devices. In the case of three level neutral point clamped inverter, there are four switching devices in one leg. but in the case of five level NPC ,there are eight switching devices per leg. Both V_{oe} and V_{no} are ac voltages. V_{oe} depends on the connection and grounding of the input AC source [2]. If the input ac source is in the Y-connection and the neutral point of the Y-connection is grounded, then V_{oe} is almost equal or close to the sinusoidal voltage .In such a case frequency is three times the frequency of the input ac source and if the input ac source is in the delta-connection and any one corner of the delta-connection is grounded, then V_{oe} will have twice higher peak value but twice lower frequency [2]. Vno is closely related inverter leg output voltage (V_{oo}, V_{bo}, and Vco)as

$$V_{no}=(V_{ao}+V_{bo}+V_{co})/3 \qquad (1)$$

Where $V_{a0,}V_{bo,}V_{co}$ are the inverter leg output voltages

II. Common-Mode Voltage Production In Variuos Neutral-Point Clamped Inverter

Since each inverter leg output voltage is a PWM modulated step-wise voltage. If represented with Fourier transform, such a voltage contains the fundamental voltage and different harmonic terms, including the harmonics at the carrier frequency, multiples of the carrier frequency, and multiples of the fundamental frequency. When a high speed pulse width modulation applied to ac motor drives, many problems such as motor bearing current, insulation breakdown, and motor leakage current have been occurs [2].The harmonics around the carrier frequency and multiples of the carrier frequency and fundamental frequency undergoes step-change ,that are blamed for the electromagnetic interference (EMI) problem. As a result, Vno contains many harmonics even though it is a step wise voltage.

V_{ne} contains harmonic voltage because it comes from both V_{no} and. V_{oe}. d Many of the harmonics in Vne can couple through stray capacitances in the motor, such as the stray capacitance between the stator winding and the grounded stator core, the stray capacitance between the stator winding and the rotor core, and the stray capacitance between the inner race of the bearing and the grounded stator core, to cause a voltage across the bearing and hence a current through the bearing. Such a bearing current can affect the properties of the bearing lubricant and cause bearing electro erosion. Different harmonics in V_{ne} can also cause a current to flow through the stray capacitance between the stator winding and the grounded stator core and other ground conductors. As a result of this, trip the ground current relays that are used to protect the drive.

The common-mode voltage and its associated dv/dt, generate

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bearing currents. Different mechanisms can be assigned to the generation of different types of bearing currents. Bearing currents can be summarized into four different currents according to their generation mechanism. The different bearing current can be summarized in to 1.Capacitive bearing current 2. Machine discharge bearing current 3. Shaft bearing current e.t.c
A solution to the CMV problem is to use filters but it is not an effective method. So it requires modifications of the PWM control strategy. However, the filters increase the size, weight, and cost of the drive, it can be used for certain applications.
The other solution is to modify the PWM control strategy to reduce the CMV Vne. Since Voe depends on the connection and grounding of the input ac source, the proposed solutions focus on using modified PWM control strategies to reduce $V_{no.}$ The solutions use a modified space vector PWM (SVPWM) scheme to reduce Vno. An SVPWM scheme having the advantages of the fact that the output voltage of an inverter leg only has three levels (VDC/2, 0, -VDC/2) or it have three states (denoted as "1," "0," and "—1," respectively), and therefore, the inverter only has 33 = 27 possible states or space vectors. The vector diagram of three level NPC is shown in the figure2. The conventional SVPWM (C-SVPWM) scheme, which uses all 27 space vectors to synthesize the reference voltage vector, this solution uses only 19 switching states to synthesize the reference space vector. The other eight switching states that lead to large ($\pm V_{DC}/3$ or $\pm V_{DC}/2$) Vn o , i.e., (1,1,0), (1,0,1), (0,1,1), (—1, —1,0), (—1,0, — 1), (0, —1, —1), (1,1,1), and—1, —1, —1), are discarded. The method reduces the magnitude of V_{no} to $V_{DC}/6$ from $V_{DC}/2$ in the C-SVPWM. Which actually limit its effectiveness in reducing the common-mode current in the 150 KHz-30 MHz frequency range for the electromagnetic compatibility (EMC)

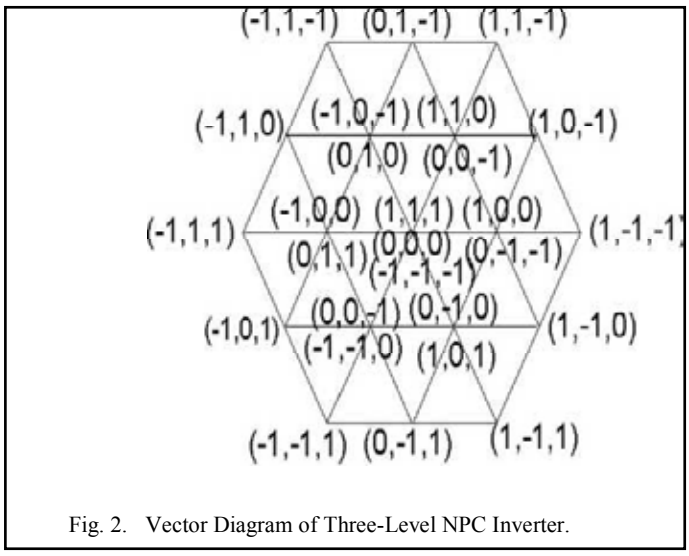

Fig. 2. Vector Diagram of Three-Level NPC Inverter.

standard in conducted emissions. The solution proposed in [11] uses only 7 out of the 27 space vectors, i.e., (0,1,-1), (1,0, —1), (1, —1,0), (0, —1,1), (—1,0,1), (—1,1,0), and (0,0,0), to synthesize the reference vector. Since each of the seven space vectors leads to zero motor neutral point to dc-link mid-point voltage V_{NO}, the method can tremendously reduce the CMV. However, the method has reduced modulation index (up to 1 rather than 1.15 in a C-SVPWM) and harmonic performance. A revised carrier-based PWM is also introduced to reduce the CMV. The method uses three balanced sinusoidal modulation signals, i.e., V_{mi}, V_{m2}, and V_{m3}, to compare with then carrier signal to yield three intermediate PWM signals Vi, V2, and V3. Here the carrier is the triangular signal. Then, the method uses (Vi — V2), (V2 — V3), and (V3 — Vi) as the PWM signals for the three phases of the inverter. As a result, the motor neutral point to dc-link mid-

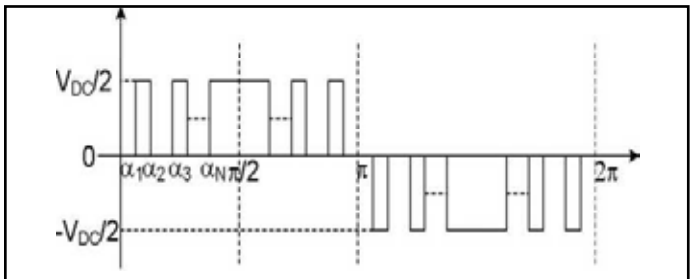

Fig. 3. Typical quarter-wave symmetric output voltage of a three-level NPC inverter leg.

point voltage is [(Vi — V2) + (V2 — V3) + (V3 — Vi)]/3 = 0.Even though this method having such advantages, the method also has reduced modulation index (up to 0.87). There is another revised carrier-based PWM is proposed and the method uses the discontinuous PWM and synchro-nized switching to reduce the number of commutations for the inverter and therefore the number of Vno pulses in one switching period. As a result, the method reduces the common-mode current in different ranges such as 150 KHz-30 MHz frequency range for the EMC standard in conducted emissions. However, the method does not reduce the magnitude of Vno which limits its effectiveness in reducing the magnitude of the common-mode current at lower frequency. The above mentioned PWM schemes for CMV or common-mode current reduction are based on SVPWM or carrier-based PWM. The use of another popular and different PWM scheme, selective harmonic elimination PWM (SHEPWM), for CMV or common current reduction in different-level NPC inverters, has not been adequately explored. The advantages of SHEPWM include direct control over output harmonics reduction of switching frequency and therefore switching loss, possibility of over-modulation, high power quality, common-mode voltage reduction and we can control the inverter at higher frequencies and also at lower frequencies.
This paper investigates the use of SHEPWM for CMV reduction in different level NPC inverters. The fundamental principle of the SHEPWM scheme is discussed in Section III. The simulation results is presented in IV Section. The conclusions are drawn in Section V.

III. Proposed Shepwm Scheme

An SHEPWM scheme represents the output voltage of each inverter leg output voltage with a Fourier series and the inverter leg output voltage shapes properly, so that unwanted harmonics are eliminated from the Fourier series. SHEPWM scheme usually shapes the output voltage of each inverter leg into a quarter-wave symmetric waveform, As a result of this even harmonics are eliminated from the Fourier series

in Fig. 3, where $\alpha 1$, $\alpha_{2,an}$ are the phase angles in a fundamental cycle where the inverter leg is switched or it is commutated. The Fourier series of such a voltage is given as

$$V_{xo} = \sum_{m=1}^{\infty} dm \sin(mwt), \quad m = 1, 2, 3, \ldots \quad (2)$$

Where V_{xo} is the output voltage of an inverter leg, x = a, b,or c; d_m is

Given as

$$dm = \begin{cases} 0, & \text{when m is even} \\ 2V_{DC}/m\pi, & \text{when m is odd} \end{cases} \quad (3)$$

i.e. by putting a,b,c ,voltage at different phase can be found out. An SHEPWM scheme should require proper value of $\alpha 1$, α_2, α_n values to eliminate selected odd harmonics from the Fourier series. For example, if the 5th, 7th, 11th, and 13th harmonics are to be eliminated, d_5, d_7, d_{11}, and d_{13} can be calculated according to (3) as

$$d_5 = 2V_{DC}/5\pi \sum_{k=1}^{N}(-1)^{K+1}\cos(5\alpha_k) \quad (4)$$

$$d_7 = 2V_{DC}/7\pi \sum_{k=1}^{N}(-1)^{K+1}\cos(7\alpha_K) \quad (5)$$

$$d_{11} = 2V_{DC}/11\pi \sum_{k=1}^{N}(-1)^{K+1}\cos(11\alpha_K) \quad (6)$$

$$d_{13} = 2V_{DC}/13\pi \sum_{k=1}^{N}(-1)^{K+1}\cos(13\alpha_K) \quad (7)$$

The resultants d_5, d_7, d_{11}, and d_{13} are then set to zero to yield the following equations

$$2V_{DC}/5\pi \sum_{k=1}^{N}(-1)^{K+1}\cos(5\alpha_k) = 0 \quad (8)$$

$$2V_{DC}/7\pi \sum_{k=1}^{N}(-1)^{K+1}\cos(7\alpha_K) = 0 \quad (9)$$

$$2V_{DC}/11\pi \sum_{k=1}^{N}(-1)^{K+1}\cos(11\alpha_K) = 0 \quad (10)$$

$$2V_{DC}/13\pi \sum_{k=1}^{N}(-1)^{K+1}\cos(13\alpha_K) = 0 \quad (11)$$

These equations can be solved by various iterative methods like Newton Raphson method. In addition to this method, other methods can also be used to get the final iterated value. By using the above method most proper value of α can be found out.

Commonly used SHEPWM scheme, includes C-SHEPWM, eliminates (6* ± 1) i.e. the (5th, 7th, 11th, 13th ...) harmonics, while keeping triplen harmonics in each inverter leg output voltage. This C-SHEPWM scheme has an advantage of the fact that the triplen harmonics, though existing in the inverter leg output voltage, will be cancelled in the line-to-line voltage of the motor. Because of the presence of the third harmonic in each inverter leg output voltage, there exist the common mode voltage similar to carrier-based PWM with the third harmonic injection .But this SHEPWM scheme has a high modulation index of 1.15. Hence it helps to control the inverter at higher frequencies.

Another important SHEPWM, called the modified SHEPWM or M-SHEPWM eliminates (4* ± 1) ie the (3rd, 5th, 7th, 9th ...) harmonics. Since this SHEPWM scheme eliminates low-order triplen harmonics from each inverter leg output voltage, it reduces the CMV of the inverter. The modified SHEPWM is actually a modification of the conventional SHEPWM technique But it has reduced modulation index (up to 1) because of absence of the third harmonic in each of the three phase

Table 1: Features of C-SHEPWM and M-SHEPWM

	C-SHEPWM	M-SHEPWM
Harmonics eliminated	6K±1	4K±1
Maximum modulation index	1.15	1
Highest harmonic order eliminated	3N- 2	2N- 1

inverter leg output voltage. Also, the highest harmonic term that can be eliminated in M-SHEPWM is lower than in C-SHEPWM. Hence it helps to control the inverter at lower frequencies .The features of C-SHEPWM and M-SHEPWM are summarized in Table I.

This paper takes advantage of the features of both the C-SHEPWM and the M-SHEPWM. The proposed SHEPWM uses the C-SHEPWM to control the inverter at high frequency (> 0.9 motor rated frequency) and the M-SHEPWM at low frequency. As a result, at high frequency, the proposed SHEPWM provides high mod-ulation index and therefore high voltage for the motor, which is necessary for high-frequency (high-speed) operation of the motor. Though the C-SHEPWM produces higher CMV, since the operating frequency and therefore the frequency of the CMV is high, a low-pass filters that consists of inductors and capacitors. Inductor in series with the motor and capacitors in parallel with the motor can effectively suppress the CMV or common-mode current of the motor. At low frequency, where the common-mode filter is less effective for CMV reduction, the M-SHEPWM is used to reduce the CMV. Even though the M-SHEPWM offers a reduced modulation index, such a modulation index is sufficient for low-frequency operation of the motor.

Another important advantage is that when the motor frequency crosses the boundary between the high and low frequencies, the C-SHEPWM and the M-SHEPWM will get a transition from one to the other. To ensure the smooth transition between the two SHEPWM schemes, the fundamental motor phase voltage completes a full cycle and passes the zero-crossing point when any transition occurs. This is shown in Fig. 4. The first SHEPWM (C-SHEPWM) continues to be used until the fundamental motor phase voltage completes a full cycle and passes the zero-crossing point at the moment *Ti*, after that only the second SHEPWM (SHEPWM-2) is used to run the inverter.

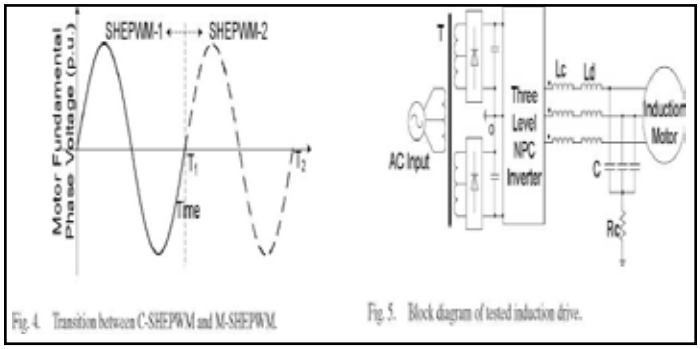

Fig. 4. Transition between C-SHEPWM and M-SHEPWM. Fig. 5. Block diagram of tested induction drive.

IV. Simulation Results

A. Simulation Diagram For Five Level NPC

Three phase five level Neutral- point clamped inverter having 8 switching devices, 8 clamping diodes and 4 dc link capacitors. The DC link capacitors have been used to divide the DC link voltage into five voltage level. Thus the name five –level.

In this work, there are eight switching devices are connected per leg. The switching signals should be synchronized with the AC supply voltage. Since the Matlab/Simulink does not have such

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triggering block set, a new triggering block has been designed and developed using the block set obtained from Simulink Toolbox. Also, the gate signals sequence and duration of conduction angle of the switches has been determined.

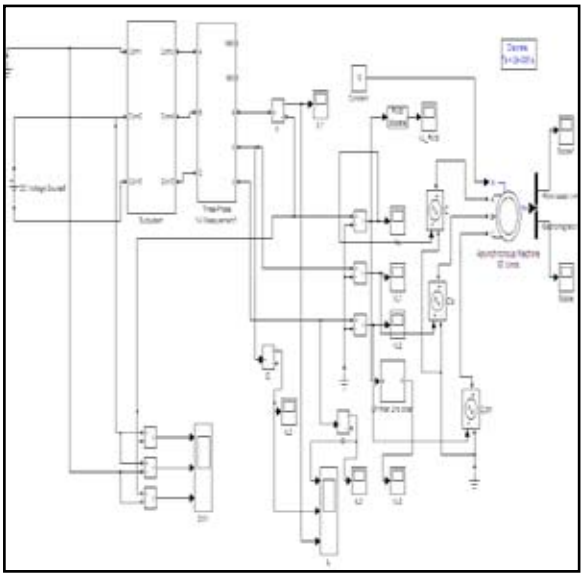

Fig 6. Simulink model for 5 level NPC

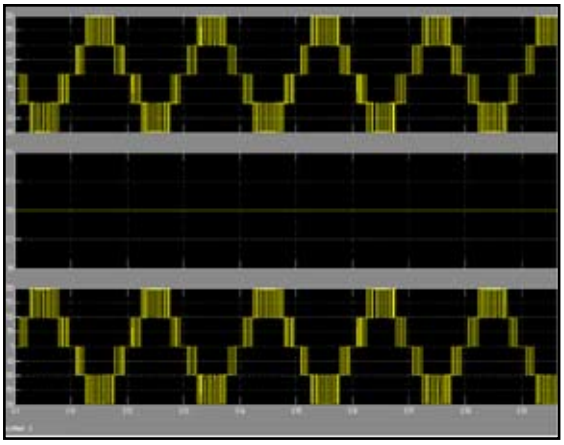

Fig 7. Common mode voltage for 5 level NPC

The current obtained from the three phases is also shown in the fig

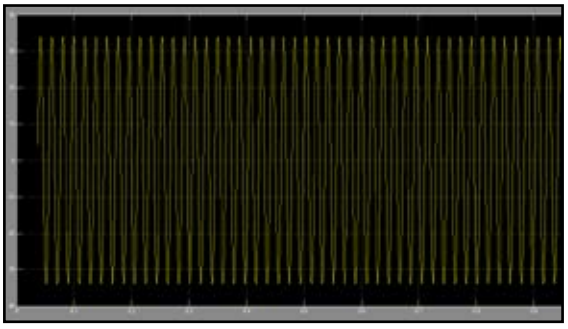

Fig . 8 : Phase current of three phase five level NPC

The THD value of all the three phase current of five level NPC is7.80%.This value is somewhat less than the THD value as obtained in the case of three level NPC

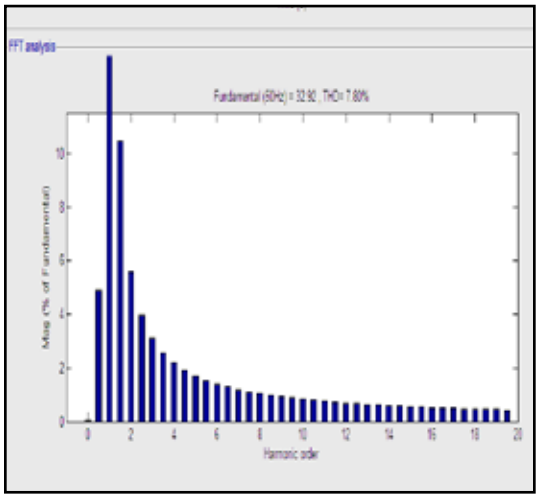

Fig. 9 : FFT analysis of three phase current of five level NPC

B. Simulation Diagram For Seven Level NPC

Three phase seven level Neutral- point clamped inverter having 12 switching devices, .12 clamping diodes and 6 dc link capacitors. The DC link capacitors have been used to divide the DC link voltage into five voltage level. Thus the name seven –level.
In this work, there are twelve switching devices are connected per leg. The switching signals should be synchronized with the AC supply voltage. Since the Matlab/Simulink does not have such triggering block set, a new triggering block has been designed and developed using the block set obtained from Simulink Toolbox. Also, the gate signals sequence and duration of conduction angle of the switches has been determined.

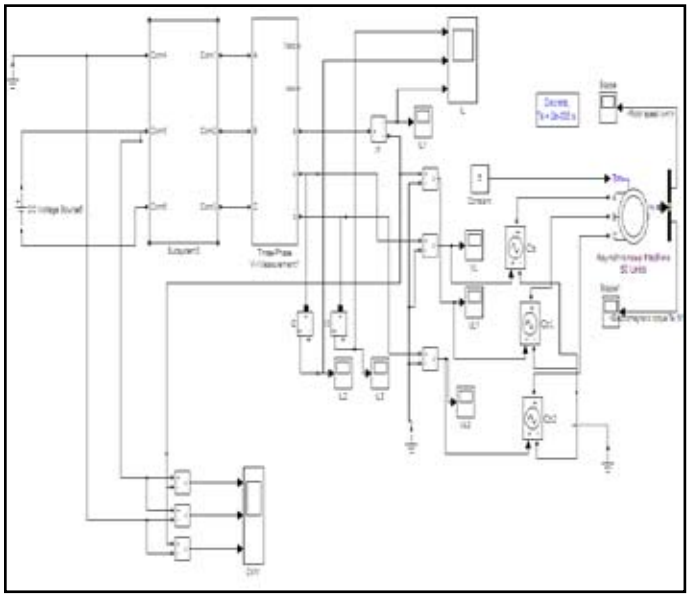

Fig 10 : Simulink model for 7 level NPC

The common-mode voltage of three phase seven level NPC is shown in the fig.11

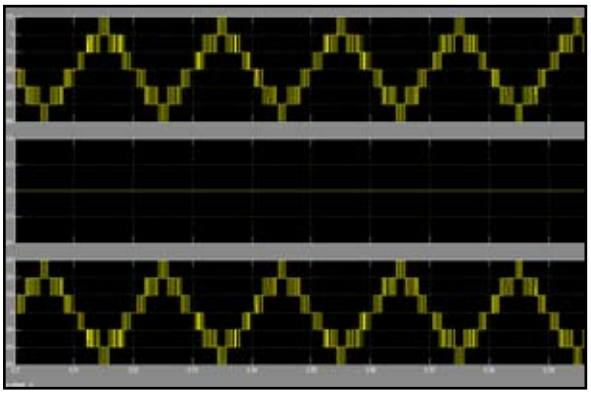

Fig.11: Common mode voltage for three phase seven level NPC

The current obtained from the three phases is also shown in the fig. The THD is actually measured for current. Compared to the five level NPC THD value is less in the case of seven level NPC and by reducing the THD value, effectively control the common-mode voltage

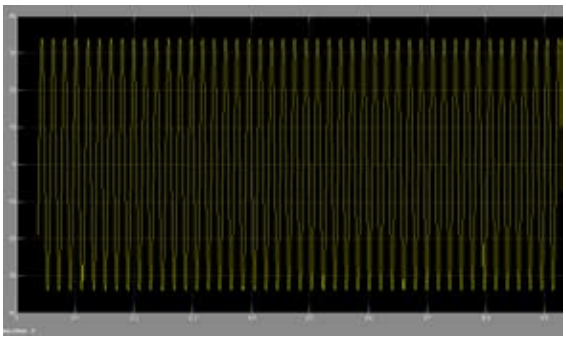

Fig .12: Phase current Ia of three phase seven level NPC

The THD value from all the three phase current of seven level NPC is 2.95%.This value is somewhat less than the THD value as obtained in the case of three level NPC

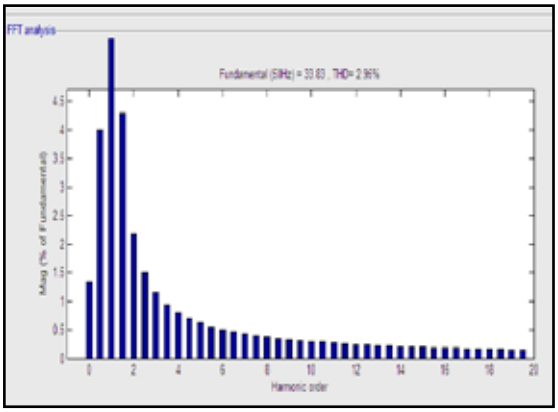

Fig.13: FFT analysis of three phase current of seven level NPC

IV. Conclusion

This paper proposed a hybrid SHEPWM scheme to reduce the CMV in a different level NPC inverter-based induction motor drive for pump and fan applications. The scheme uses the C-SHEPWM to control the inverter at high frequency and the M-SHEPWM at low frequency, to meet the modulation index and CMV requirement of the drive. Experimental results show that the proposed scheme could provide the required modulation index and effectively control the CMV at different levels. The experimental results also show that the proposed scheme could have reduced THD value. The following table shows the THD values of different levels like three, five and seven. From the table, we can understood that the THD value of seven level is less compared to three level inverter.

LEVEL	THD VALUE
1. FIVE LEVEL NPC	7.81%
2.SEVEN LEVEL NPC	2.95%

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