ISSN : 2394-2975 (Online)
ISSN : 2394-6814 (Print)

Matlab Simulation for Bridgeless Buck Converter

Niyas Thayyil
Assistant Professor

Abstract
A bridgeless buck rectifier that substantially improves efficiency at the universal line range is introduced. By eliminating input bridge diodes, the rectifier's efficiency is further improved. Moreover, the rectifier doubles its output voltage, which extends useable energy of the bulk capacitor after a dropout of the line voltage. The operation and performance of the circuit was verified in MATLAB software in 500W, 65 kHz. The simulated efficiencies at 50% load from 115 and 230V line are both closed to 96.4%.

Keywords
Bridgeless Rectification, Buck Converter, Matlab, Voltage Doubler.

Introduction

Environmental Protection Agency's (EPA) and climate saver computing Initiative (CSCI) [1] specification define minimum efficiency at 100%, 50%, and20% of full load with a maximum efficiency at 50%load. In universal- line (90-264V) applications, maintaining a high efficiency across the entire line range posses a major challenge for ac/dc rectifier. A bridge diode rectifier follower by a boost converter has been the most commonly used because of its simplicity and good power factor. However, a boost front-end exhibits 1%-3%lower efficiency at 100Vline compared to that at 230V line. Due to increased input current that produce higher looses in semiconductors and input electromagnetic interference filter components.

Drawback of universal line boost converter is high output voltage typically in the 380-400V range. It effect on the switching losses and switching losses of primary switches of the downstream dc/dc output stage and size and efficiency of a power supply exhibits falloff as the load current decreases. Below 850W, the above drawbacks demonstrated in [2]. The buck converter operation in both discontinuous current mode and continuous current mode was described in [3].

Because the buck power factor correction does not shape the line current around the zero crossings of the line voltage, i. e., during the time intervals when the line voltage is lower than the output voltage, it exhibits increased total harmonic distortion and lower power factor compare to its boost counterparts.

In this paper, a bridgeless buck rectifier that further improves the low line (115V) efficiency of the buck front end by reducing the conduction loss through minimization of the number of simultaneously conducting semiconductor components is introduced. Because the bridgeless buck rectifier also works as a voltage doubler, it can be designed to meet harmonic limit specifications with an output voltage that is twice that of ac conventional buck power factor correction rectifier. Although the output voltage doubled, the switching losses of the primary switches of the downstream dc/dc output stage are still significantly lower than that of the boost power factor correction counterparts,

It should be noted that a bridgeless voltage doubler boost topology has been introduced in [4]. However, because this topology operates with the output voltage higher than twice the peak input voltage, i.e., with an output voltage of around 800V, its employment in universal- line applications is not practical with high–voltage semiconductor switches available today. Specifically, high- voltage silicon insulated gate bipolar transistors and MOSFETs with voltage rating in the 1000-1200V range that are required to implement this topology in universal – line applications exhibit increased losses and are more expensive than their counterparts rated at 600V and below. In fact, the bridgeless voltage doubler boost rectifier topology will become attractive from a performance point of view once high voltage SiC and GaN device become available in the future.

To verify the operation and performance of the bridgeless buck rectifier, a 200W, universal line experimental prototype operating at 65 kHz was build in Matlab software. The simulated result contained efficiency at 50%load over the input voltage range from115 to230V is more than 96%.

II. Bridgeless Buck Rectifier With Voltage Doubler Circuit

The propose bridgeless buck rectifier, as shown in Fig. 1, employs two back to back connected buck converters that operate in alternative halves of the line voltage cycle. The buck converter illustrated in Fig. 2 only operate during positive half-cycles of line voltage V_{ac} and consists of a unidirectional switch implemented by diode D_1 in series with switch S_1, freewheeling diode D_3, filter inductor L_1, and output capacitor C_1. During its operation, the voltage across capacitor C_1, which must be selected lower than the peak of line voltage, is regulated by pulse width modulation of switch S_1.Similary, the buck converter consisting of the unidirectional switch implemented by diode D_2 in series with the switch S_2, freewheeling diode D_4, filter inductor L_2, and output capacitor C_2 operate only during negative half cycles of line voltage V_{ac}, as shown in Fig. 3. During its operation, the voltage across capacitor C_2 is regulated by the pulse width modulation of switch S_2

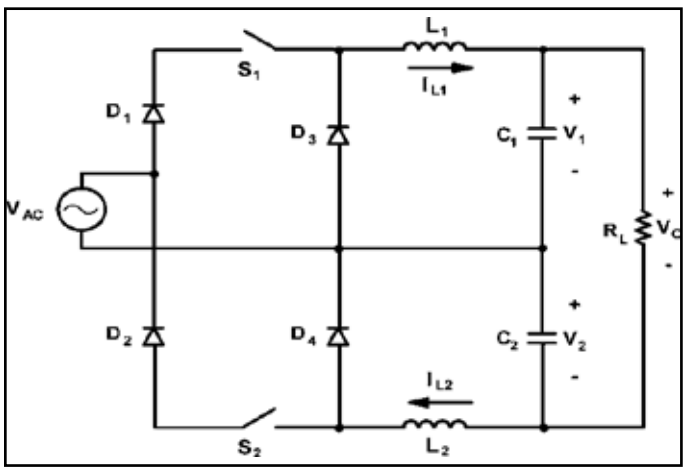


Fig. 1 : Bridgeless buck rectifier.

© IJARET All Rights Reserved

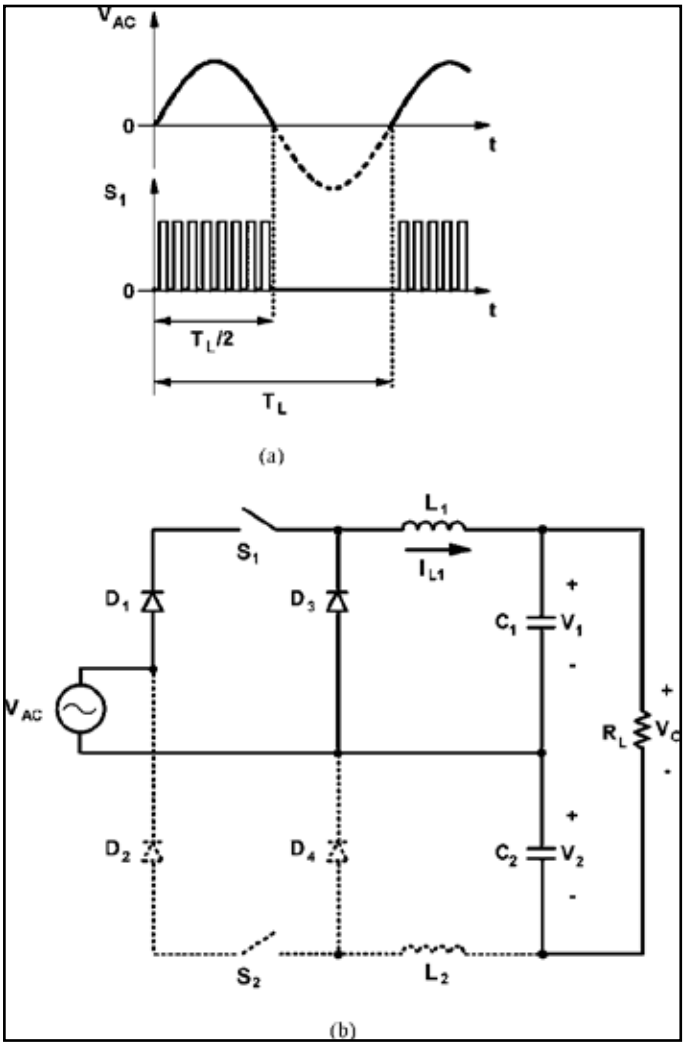
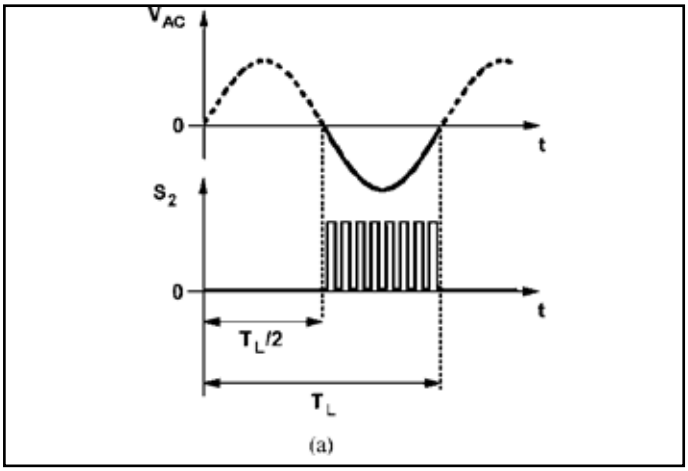


Fig. 2 : Operation of the bridgeless buck rectifier during the period when the line voltage is positive.

As seen from Figs. 2 and 3, the input current always flows through only one diode during the conduction of a switch, i.e., either D_1 or D_2. Efficiency is further improved by eliminating input bridge diodes in which two diodes carry the input current. Advantage of circuit is its inrush current control capability. Since the switches are located between the input and output capacitors, switches $S_1$and S_2 can actively control the input inrush current during start-up.



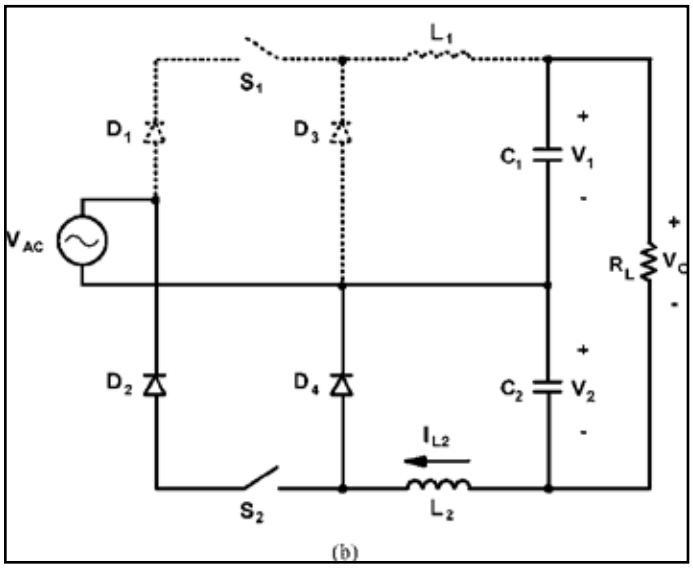


Fig . 3 : Operation of the bridgeless buck rectifier during the period when the line voltage is negative.

Output voltage $V_{out\ of}$ the bridgeless rectifier, which is the sum of the voltage across capacitors$C_1$and C_2, is given by

$$V_{out} = 2DV_{in} \quad (1)$$

Where D is the duty cycle and V_{in} is the instantaneous rectified ac input voltage. Because of the buck topology, the relationship shown in (1) is valid for input voltage V_{in} greater than half the output voltage, i.e., for $V_{in} > V_{out}/2$. When input voltage V_{in} falls below $V_{out}/2$, the converters do not Deliver energy from the input to the output so the load current is maintained solely by the output capacitors.

The time the buck converter does not operate during a half-line cycle. It was found that for power levels below 850 W, output voltage should be kept below 160 V to meet the IEC61000-3-2 harmonic requirements. It should also be noted that the switching losses of the proposed rectifier is significantly low, because the rectifier does not operate during the time when the input voltage is lower than half the output voltage.

III. Simulation Results

MATLAB is a high-level language and interactive environment for numerical computation, visualization, and programming. Using MATLAB, you can analyze data, develop algorithms, and create models and applications. The language, tools, and built-in math functions enable you to explore multiple approaches and reach a solution faster than with spreadsheets or traditional programming languages, such as C/C++ or Java.

Bridgeless Buck rectifier in MATLAB/Simulink software is implemented. Regulator and filter required at the outputs in order to obtain correct waveforms and visualize the fundamental results. Our simulation analysis does not include the programming of dead time for the switching of complementary switches in a converter.

© IJARET All Rights Reserved

ISSN : 2394-2975 (Online)
ISSN : 2394-6814 (Print)

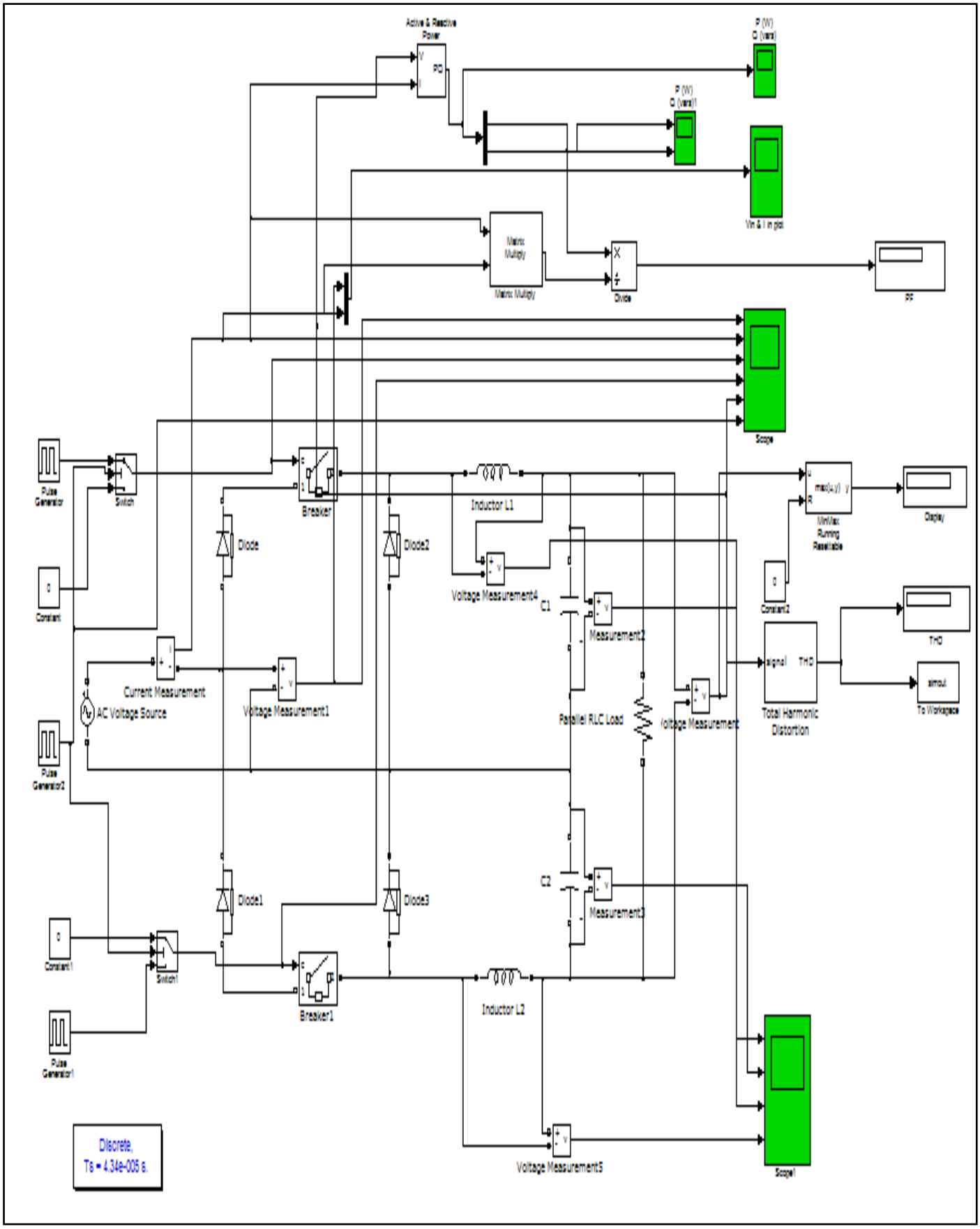


Fig. 4 : Bridgeless buck rectifier System Model.

© IJARET All Rights Reserved

IV. Simulated Input Voltage And Current Waveforms

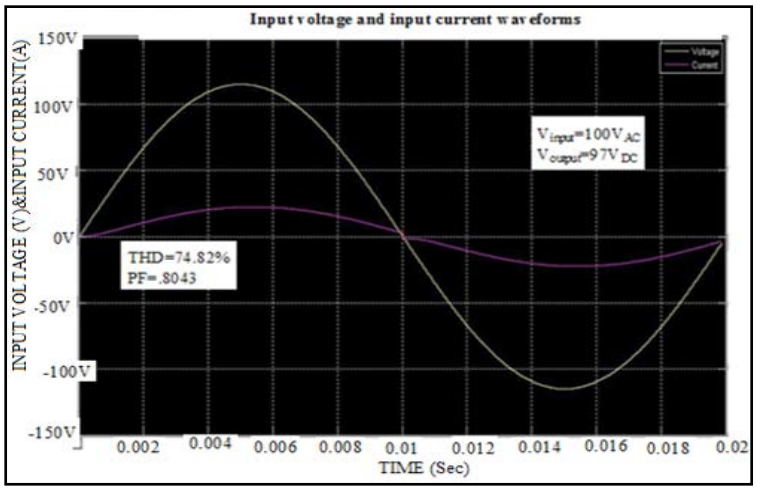


Fig 4.1 : Input voltage and input current waveforms

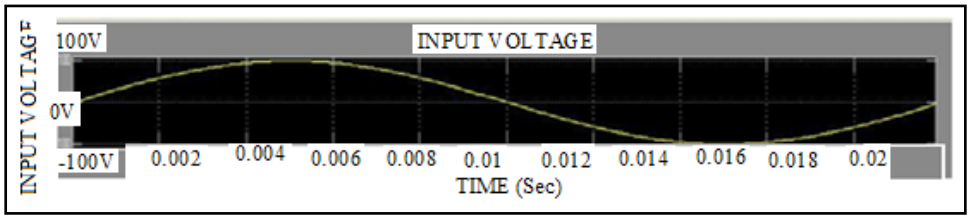


Fig.4. 2 : Input voltage

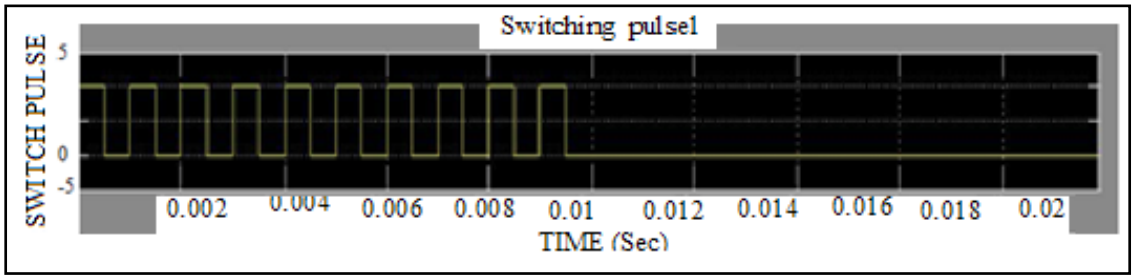
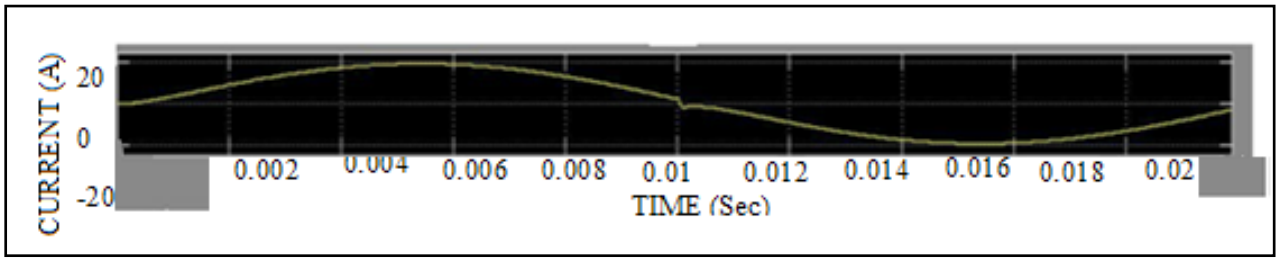
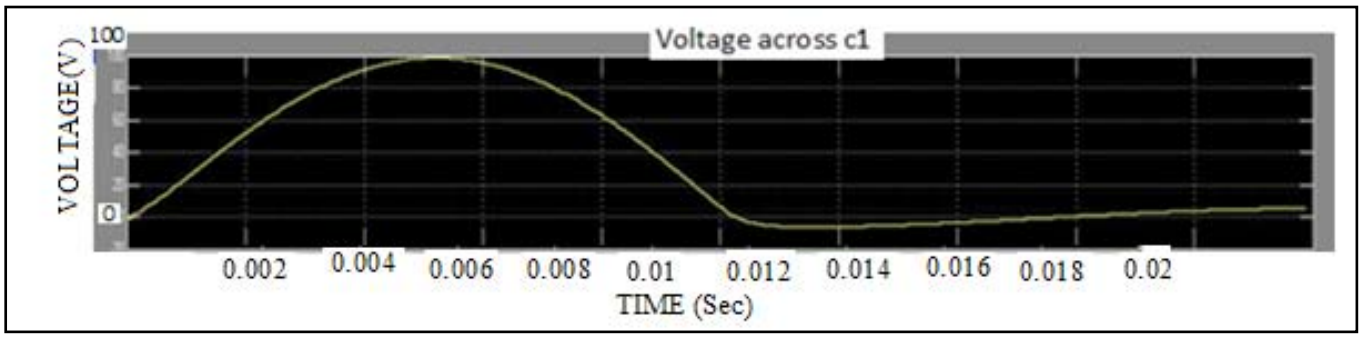


Fig.4. 3 : Switching pulse 1

4.4 : Switching pulse 2



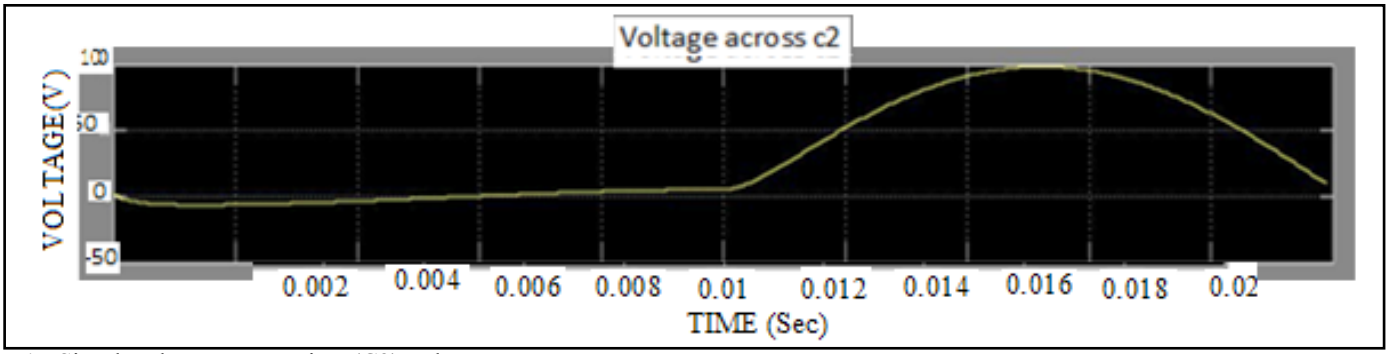
V. Input Voltage, Input Current, Output Voltage And Switching Pulse Waveforms



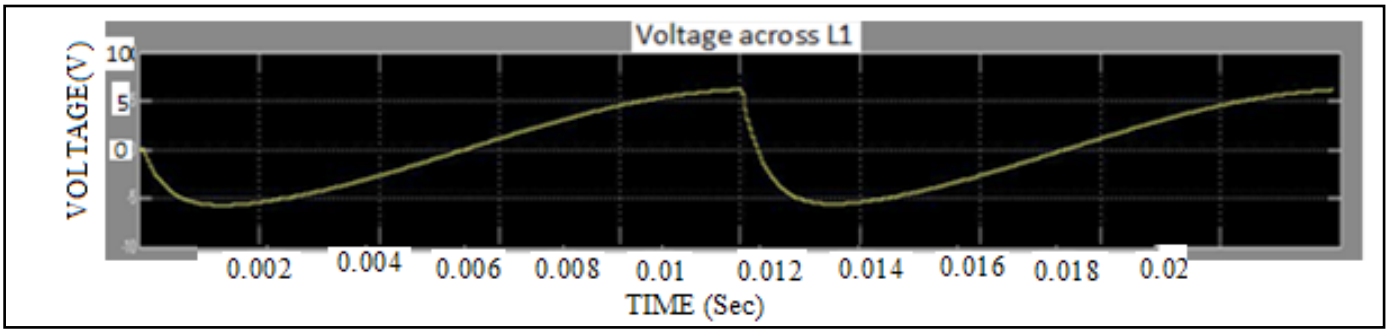
5.1 : Simulated output capacitor (C1) voltages

© IJARET All Rights Reserved

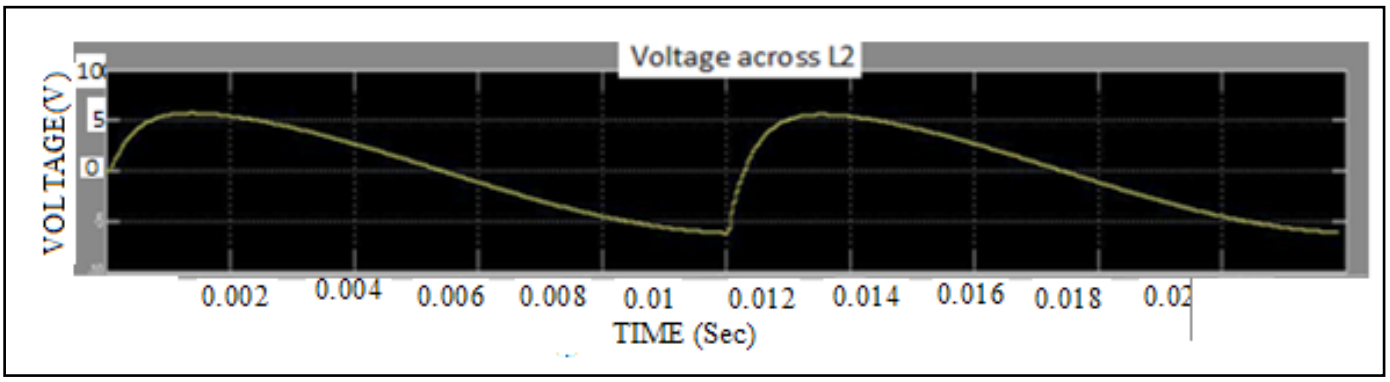
ISSN : 2394-2975 (Online)
ISSN : 2394-6814 (Print)



5.1 : Simulated output capacitor (C2) voltages



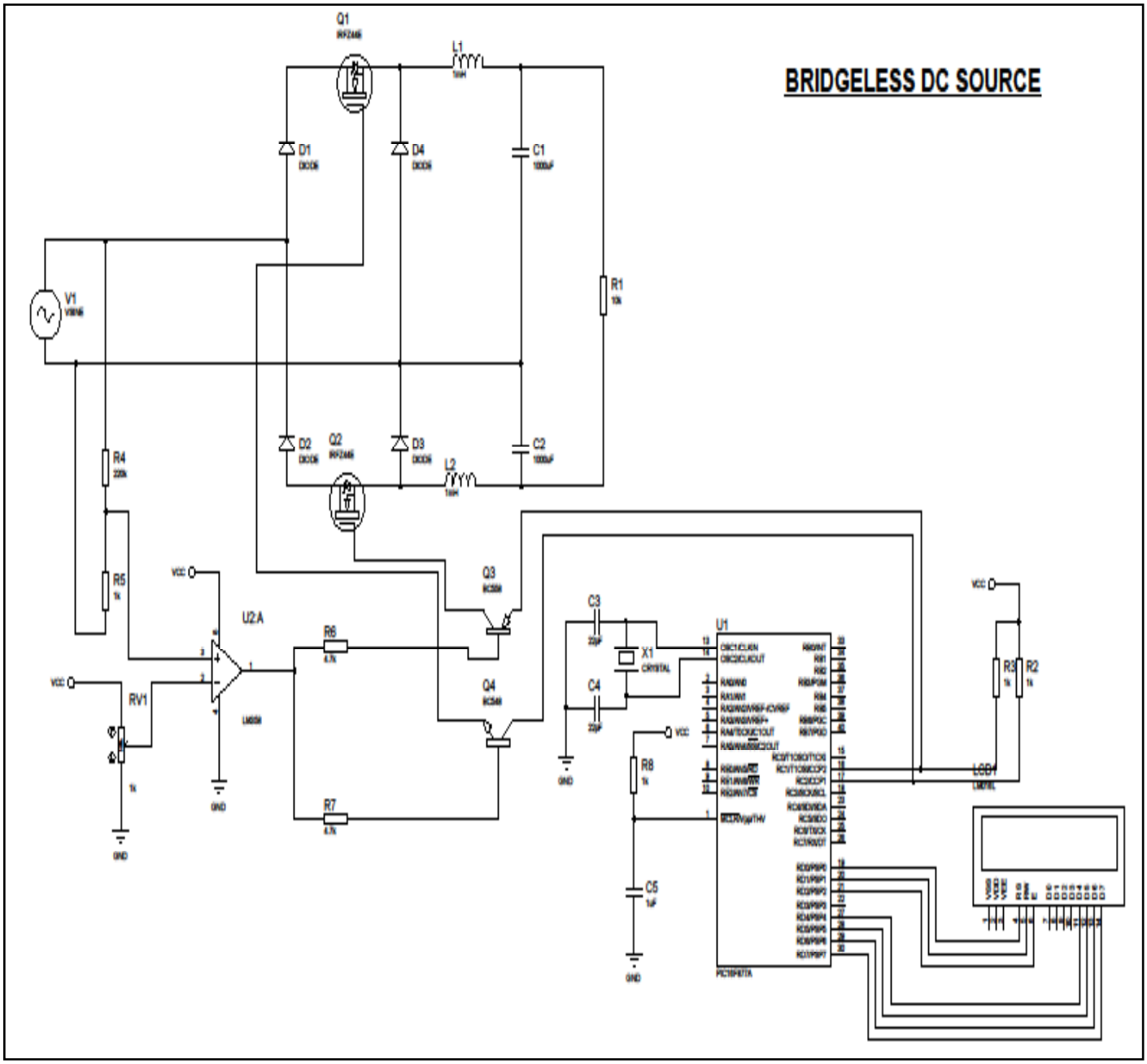
5.2 : Simulated output capacitor (L2) voltages



5.3 : Simulated output capacitor (L2) voltages

© IJARET All Rights Reserved

VI. Experimental Result



© IJARET All Rights Reserved

ISSN : 2394-2975 (Online)
ISSN : 2394-6814 (Print)

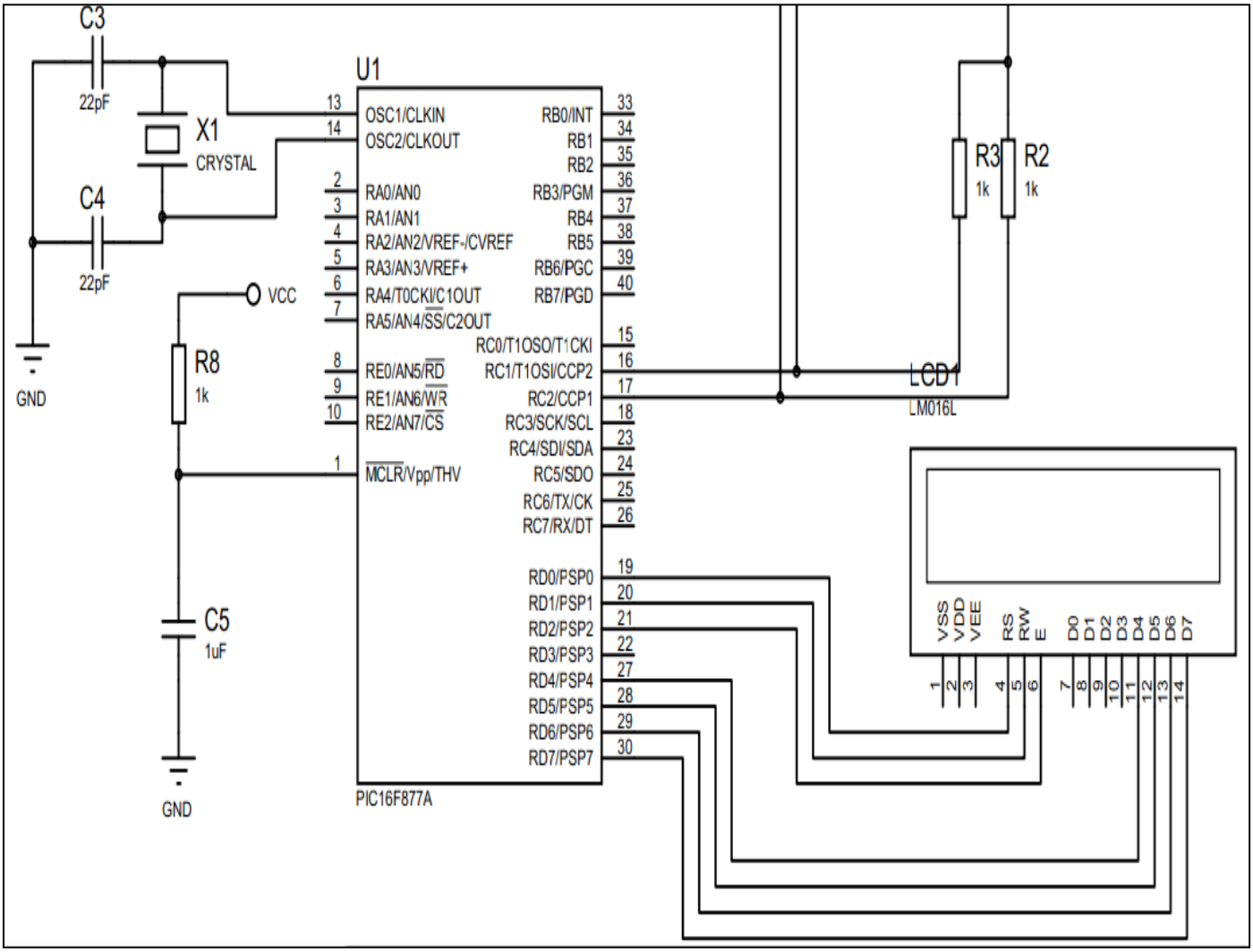


Fig. 6 : Experimental prototype circuit of the bridge less buck rectifier

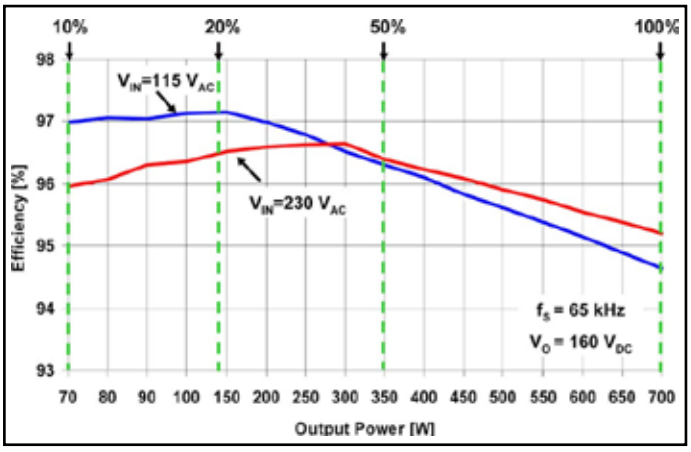


Fig. 6.1 : Measured efficiency of the the bridge less buck rectifier

The performance of the rectifier in–Fig. 6 was evaluated on a 65-kHz, 200-W prototype circuit that was designed to operate from a universal ac-line input (85-256 V_{RMS}) with a 160 V output. Fig. 6 shows the schematic diagram and component details of the experimental prototype circuit. Since the voltage of switches Q_1 and Q_2 are clamped to the voltage difference between the input voltage and output capacitor voltage, the peak voltage stress on switch Q_1 and Q_2 can be as high as 380 V, which is the peak input voltage at the maximum line. The peak current stress on switch Q, which occurs at full load and low line, is approximately 9 A. Therefore, a IRFZ44E was used for each buck switch. Since buck diodes D3 and D4 must block both the same peak voltage stress and conduct the same peak current as the switches, an diode was used.

It should be noted that in the universal-input bridgeless buck rectifier there is no need to use SiC diode as in its boosted counterparts since the reverse recover related losses in the buck PFC are lower than those in the boost PFC. Because the reverse- recovery-related losses are given by the product of reverse- recovery charge Q_{RR} of the diode, the reverse voltage across the diode, and switching frequency f_S, these losses are lower in the buck PFC rectifier than in the boost because the reverse voltage across the diode is much smaller in the buck PFC rectifier. Whereas in the boost PFC the reverse voltage across the boost rectifier is equal to the output voltage, i.e., it is constant at 380– 400 V, in the buck PFC the reverse voltage across the buck diode is given by the input voltage, which varies from zero to the peak of the line. At low line of 85_{VRMS}, where the reverse-recovery losses are the greatest, the reverse voltage across the buck diode varies from 0 to $85 \times 1.414 = 120$ V, which is much smaller than that in its boost counterpart.

To obtain the desired inductance of output inductor L_1 and L_2 of approximately 1mH and also to achieve high efficiency at light load, the output inductor was built using a pair of ferrite cores. Litz wires were employed to reduce fringe effects near the gap area of the inductors. Three aluminum capacitors (1000 uF, 100 VDC)

© IJARET All Rights Reserved

were used for output capacitors C_1 and C_2 for their ability to meet the hold-up time requirement (20 ms at 50% load and 12 ms at full load. The bulk capacitor voltage that is the voltage across series connected capacitors C_1 and C_2 was regulated by a single controller. Switches Q_1 and Q_2 were operated simultaneously by the same gate signal from the PWM controller. Although both switches were always gated, only one switch carried positive current and delivered power to the output, i.e., switch Q_1 on which the positive input voltage was induced, as shown in Fig. 2. The other switch on which the negative input voltage is induced, i.e., switch Q_2 , as shown in Fig. 2, did not influence the operation since diode D_2 , which is connected in series with switch Q_2, blocked the current. It should be noted that the voltage across each capacitor *C*1 or *C*2 could also be regulated by PIC16F877A controllers. The voltage imbalance by the mismatched output inductors can be completely eliminated.

Fig.6.1 shows the measured efficiency of the proposed bridgeless buck rectifier. It should be noted that the low-line efficiency is higher than the high-line efficiency over the load range below 40%. The efficiency difference between low line and high line is less than 0.5% over the load range above 50%, which is desirable for thermal optimization.

VII. Summary

In this paper, a bridgeless buck rectifier that substantially improves the efficiency at low line has been introduced. The proposed rectifier doubles the rectifier output, which extends useable energy after a dropout of the line voltage. Moreover, by eliminating input bridge diodes, efficiency is further improved.

The operation and performance of the proposed circuit was verified on a 200-W, universal-line experimental prototype operating at 65 kHz. The measured efficiencies at 50% load from 115 and 230 V line are close to 96.4%. The efficiency difference between low line and high line is less than 0.5% at full load. Finally, a half-bridge dc/dc converter is added as a second-stage converter. The measured total efficiency is well above the CSCI specifications at both 115 and 230 V line.

Acknowledgement

The authors would like to thank my teachers and Support Engineers from the Power Electronics Laboratory, Orient Products Corporation, for their assistance in constructing the experimental converters and collecting data.

Reference

[1] *Climate savers computing initiative, white paper.(2007). [Online]. Available: http://www.climatesaverscomputing.org/docs/20655_Green_Whitepaper_0601307_ry.pdf.*

[2] *L. Huber, L. Gang , and M. M. Jovanovic, "Design-Oriented analysis and performance evaluation of buck PFC front end, "IEEE Trans. Power electron., vol.25, no.1,pp. 85-64, Jan. 2010.*

[3] *H. Endo, T. Yamashita, and T. Sugiura, "A high power factor buck converter," in Proc. IEEE power Electron. Spec. Conf. (APEC) Rec., Jun.1992, pp. 1071-1076*

[4] *J. C. Salmon, "Circuit topologies for single phase voltage doubler boost rectifiers". IEEE Trans. Ind. Appl., vol. 8, no.4, pp. 521-529, Oct. 1993.*

Author Profile

Niyas Thayyil was born in Malappuuram, Kerala, India. He received the Engineering degree in electrical engineering from the University of Calicut; He is Assistant Professor in University of Calicut.

© IJARET All Rights Reserved